APEX 20K

Programmable Logic Device Family

March 2000, ver. 2.06 Data Sheet

Features...

Preliminary Information

- Industry's first programmable logic device (PLD) incorporating system-on-a-programmable-chip integration
  - MultiCore™ architecture integrating look-up table (LUT) logic, product-term logic, and embedded memory
  - LUT logic used for register-intensive functions
  - Embedded system block (ESB) used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
  - ESB implementation of product-term logic used for combinatorial-intensive functions
- High density
  - 30,000 to 1.5 million typical gates (see Table 1)
  - Up to 51,840 logic elements (LEs)
  - Up to 442,368 RAM bits that can be used without reducing available logic
  - Up to 3,456 product-term-based macrocells

Table 1. APEX 20K Device Features *Note (1)*

Feature	EP20K30E	EP20K60E	EP20K100E EP20K100	EP20K160E	EP20K200E EP20K200	EP20K300E	EP20K400E EP20K400	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	113,000	162,000	263,000	404,000	526,000	728,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	30,000	60,000	100,000	160,000	200,000	300,000	400,000	600,000	1,000,000	1,500,000
LEs	1,200	2,560	4,160	6,400	8,320	11,520	16,640	24,320	38,400	51,840
ESBs	12	16	26	40	52	72	104	152	160	216
Maximum RAM bits	24,576	32,768	53,248	81,920	106,496	147,456	212,992	311,296	327,680	442,368
Maximum macrocells	192	256	416	640	832	1,152	1,664	2,432	2,560	3,456
Maximum user I/O pins	128	204	252	316	382	408	502	624	708	808

Note:

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

…and More Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 2)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-Vdevices (see Table 2)
  - ESB offering programmable power-saving mode
- Flexible clock management circuitry with up to four phase-locked loops (PLL)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ($\mathbf{t_{CO}} + \mathbf{t_{SU}}$) up to 370 MHz
  - LVDS performance up to 624 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 2)
  - Programmable clamp to V_{CCIO}
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), and Gunning transceiver logic plus (GTL+) and high-speed terminated logic (HSTL Class I)
  - Supports hot-socketing operation
  - Pull-up on I/O pins before and during configuration

Table 2. APEX 20K Supply Voltages

Feature	EP20K100 EP20K200 EP20K400	EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V 5.0 V *(1)*	1.8 V, 2.5 V, 3.3 V

Note:
(1) Certain APEX 20K devices are 5.0-V tolerant. See "MultiVolt I/O Interface" on page 46 for details.

- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 3 through 6)
  - FineLine BGA™ packages maximize board space efficiency
  - SameFrame™ pin migration providing migration capability across device densities and package sizes
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore™ functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools

- Quartus SignalTap™ embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20K QFP, BGA & PGA Package Options & I/O Count *Notes (1), (2), (3)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA	984-Pin PGA
EP20K30E	92	128					
EP20K60E	92	151	183	204			
EP20K100	101	159	189	252			
EP20K100E	92	151	183	246			
EP20K160E	87	143	175	273			
EP20K200		144	174	279			
EP20K200E		136	168	273	376		
EP20K300E		120	152		408		
EP20K400					502	502	
EP20K400E					488		
EP20K600E					488		
EP20K1000E					488		716
EP20K1500E					488		858

Table 4. APEX 20K FineLine BGA Package Options & I/O Count *Notes (1), (2), (3)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	108	128	128 *(4)*	128 *(4)*	
EP20K60E	108	204	204 *(4)*	204 *(4)*	
EP20K100		252	252 *(4)*	252 *(4)*	
EP20K100E	108	246	246 *(4)*	246 *(4)*	
EP20K160E			324	324 *(4)*	
EP20K200			382	382 *(4)*	
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 *(5)*	
EP20K400E				488 *(5)*	
EP20K600E				508 *(5)*	588
EP20K1000E				508 *(5)*	708
EP20K1500E					808

Notes to tables:

(1) Contact Altera for up-to-date information on package availability.
(2) I/O counts include dedicated input and clock pins.
(3) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
(4) All FineLine BGA packages, except the 144-pin and 1,020-pin packages, are footprint-compatible via SameFrame pin-out. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 45 for more information.
(5) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 5. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 6. APEX 20K FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

General Description

APEX 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to over one million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 7 summarizes the features included in APEX 20K and APEX 20KE devices.

Table 7. Comparison of APEX 20K & APEX 20KE Features

Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
Hot-socketing support	Full support	Full support
SignalTap logic analysis	Full support	Full support
64-Bit, 66-MHz PCI	Full compliance	Full compliance
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block
ClockLock support	Clock delay reduction 2× and 4× clock multiplication	Clock delay reduction $m/(n \times v)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVDS and LVPELL data pins (in EP20K300E and larger devices) LVDS and LVPELL clock pins (in all devices) LVTTL HSTL Class I LVPECL PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

Contact Altera for information on future configuration devices.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by Altera's Quartus development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus software from within third-party design tools. Further, the Quartus software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus development system, includes DesignWare functions optimized for the APEX 20K architecture.

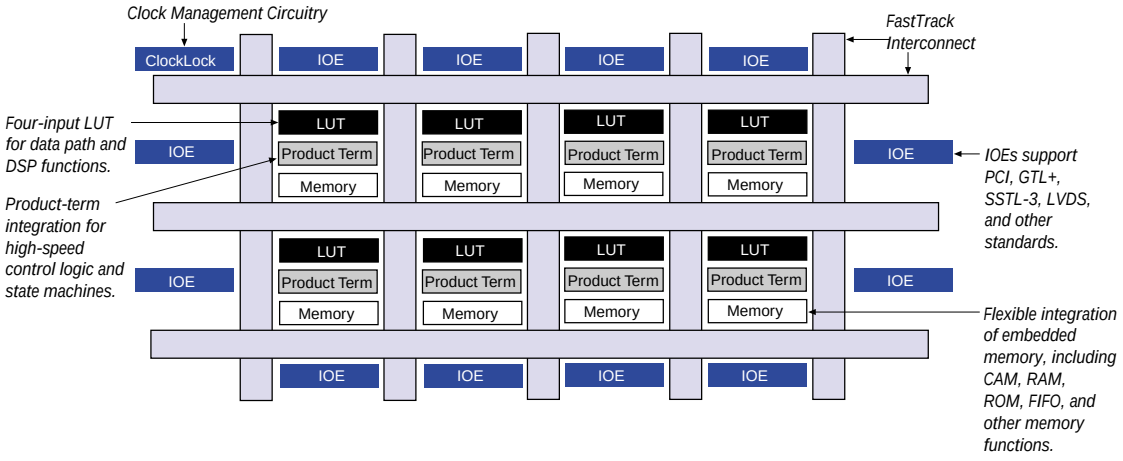
Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, HSTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, LVPELL GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram

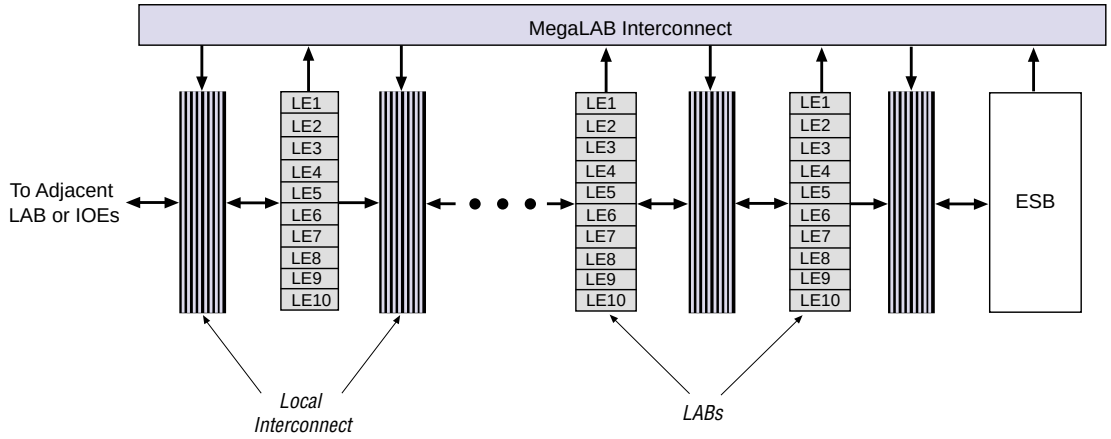


APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000E and EP20K1500E devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure

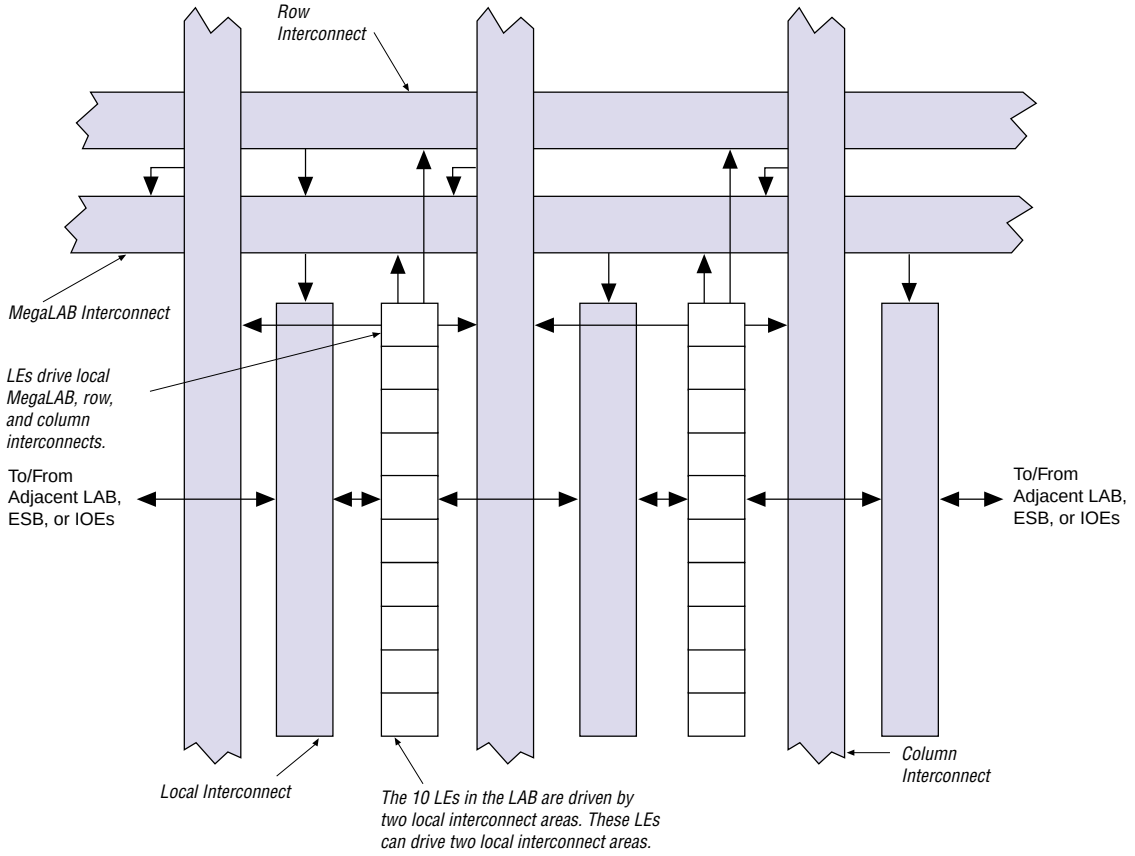


Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure



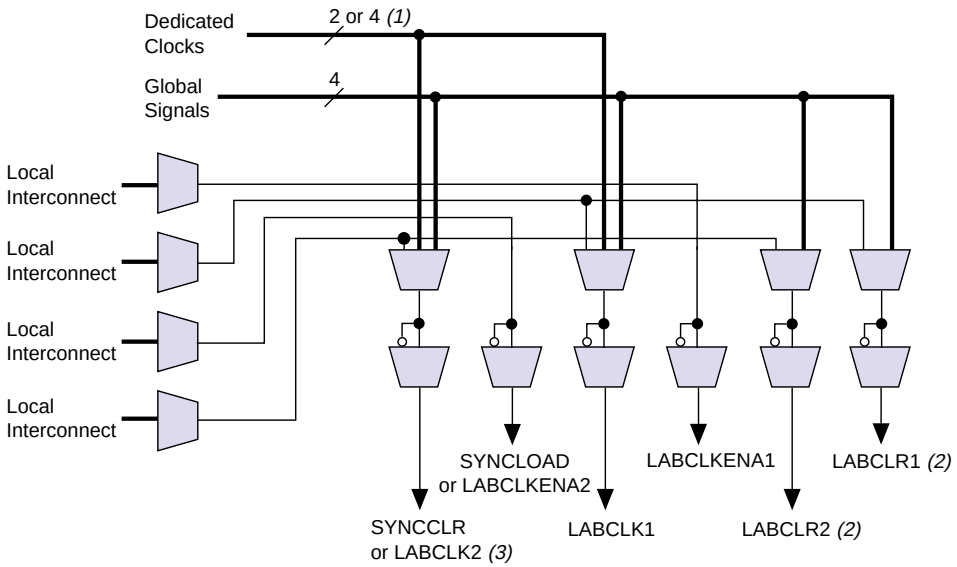
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in an LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



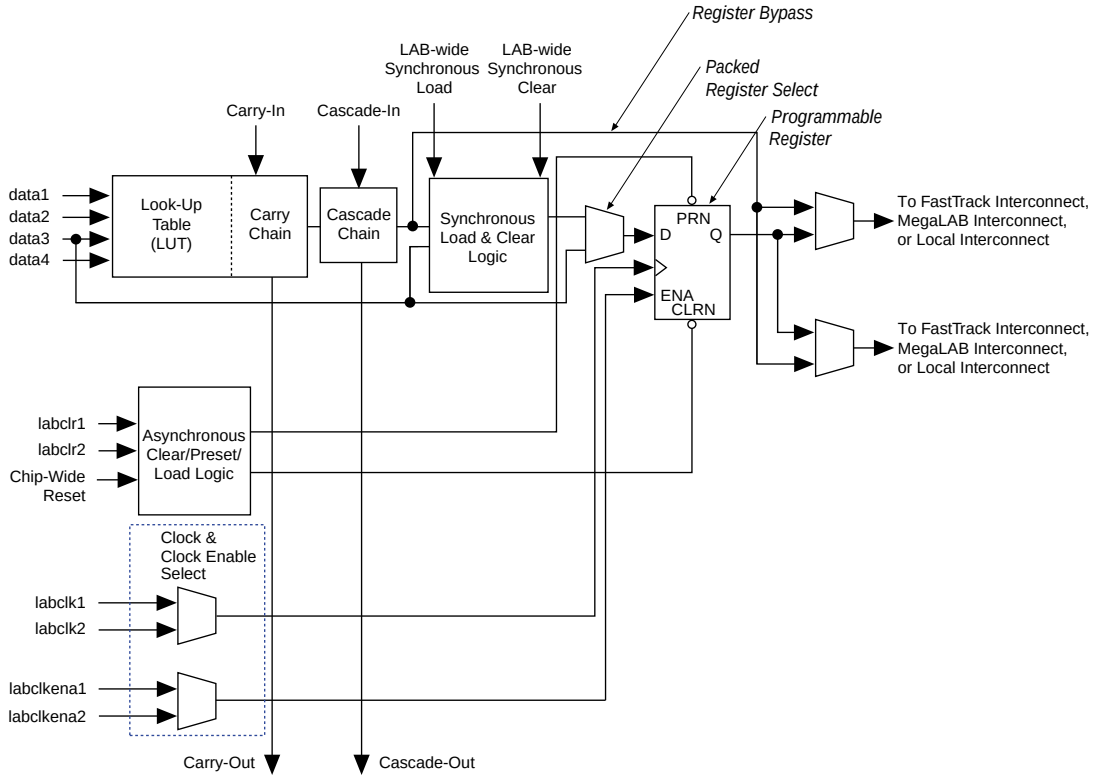
Notes:

(1) APEX 20KE devices have four dedicated clocks.
(2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
(3) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

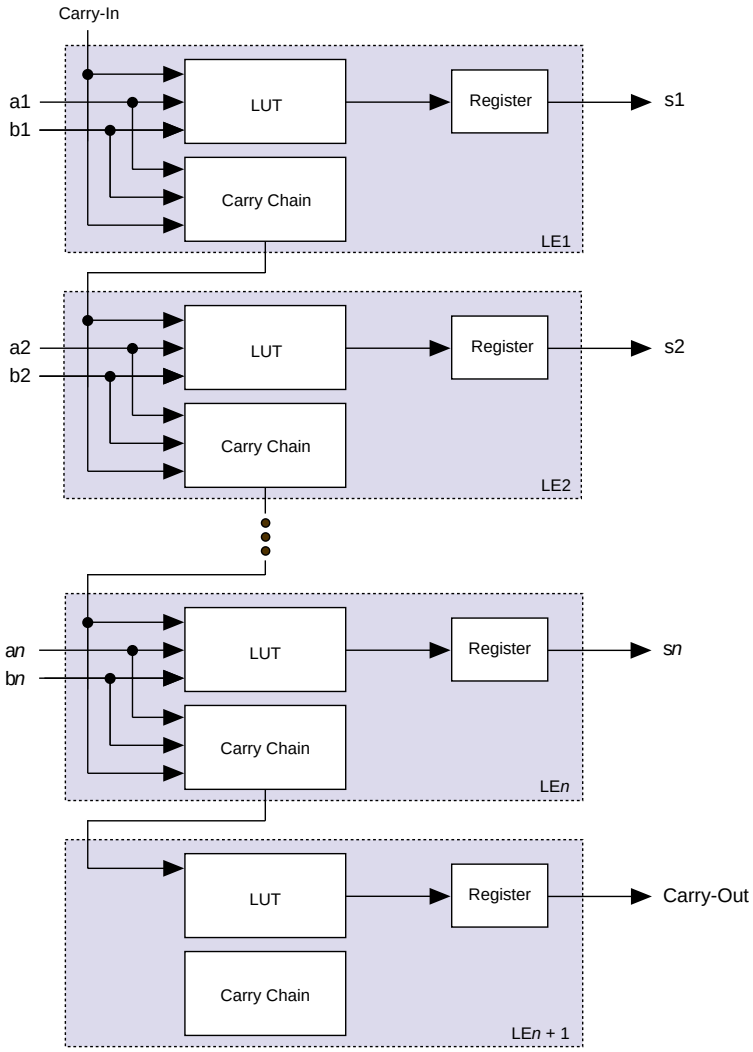
Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

Figure 6. APEX 20K Carry Chain

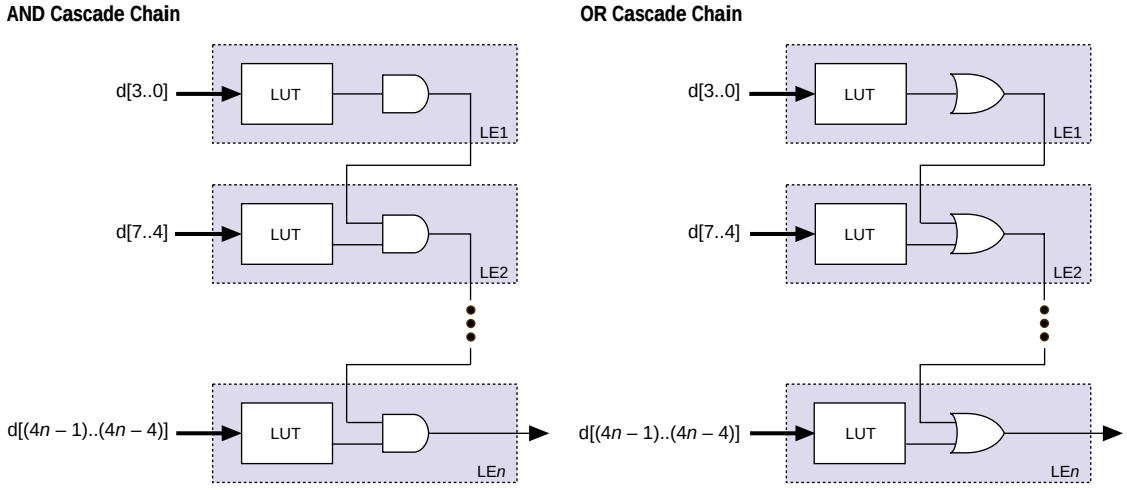


Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain



LE Operating Modes

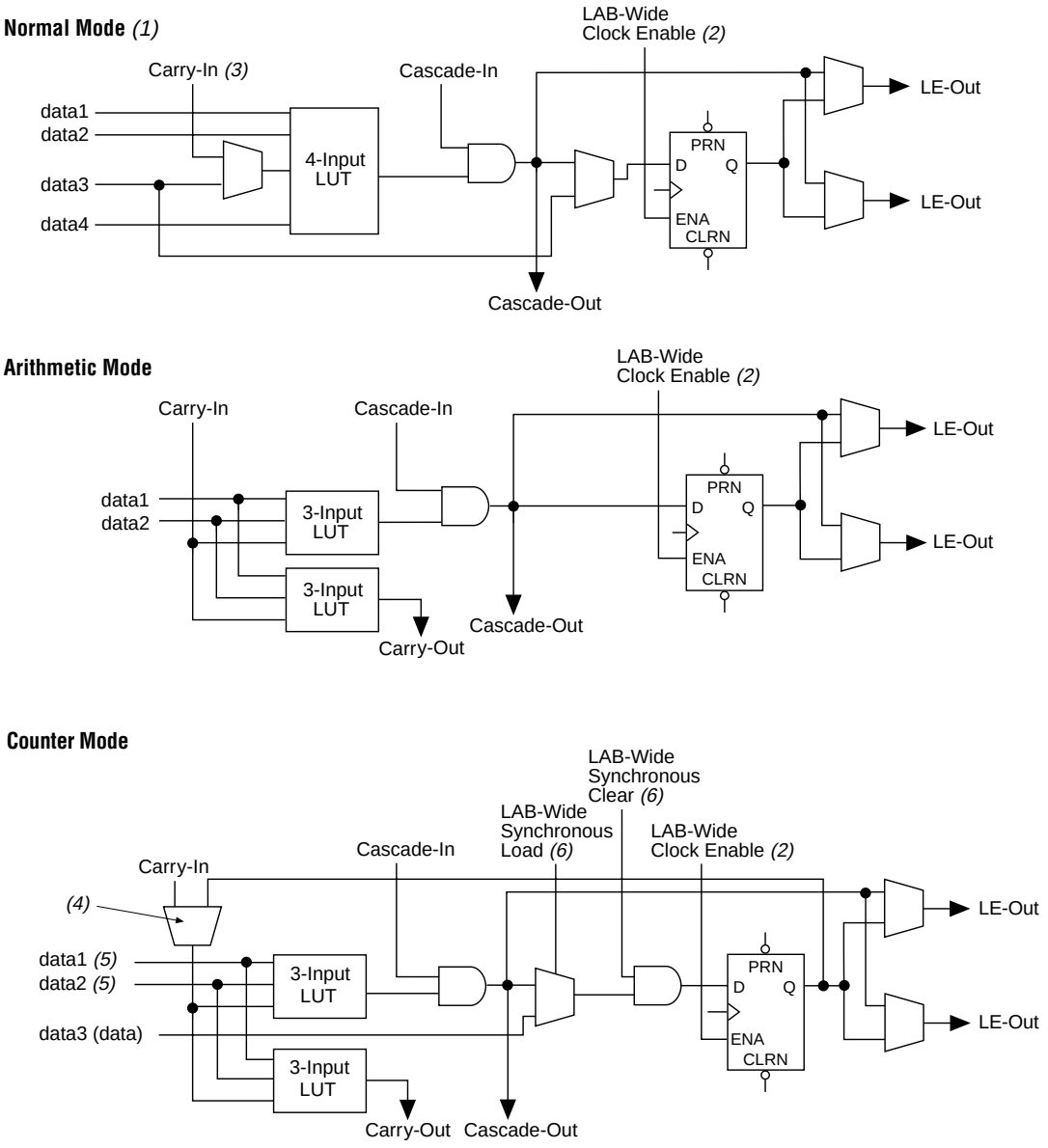
The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 8. APEX 20K LE Operating Modes



Notes:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up / down control, synchronous clear, and synchronous load options. The counter enable and synchronous up / down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

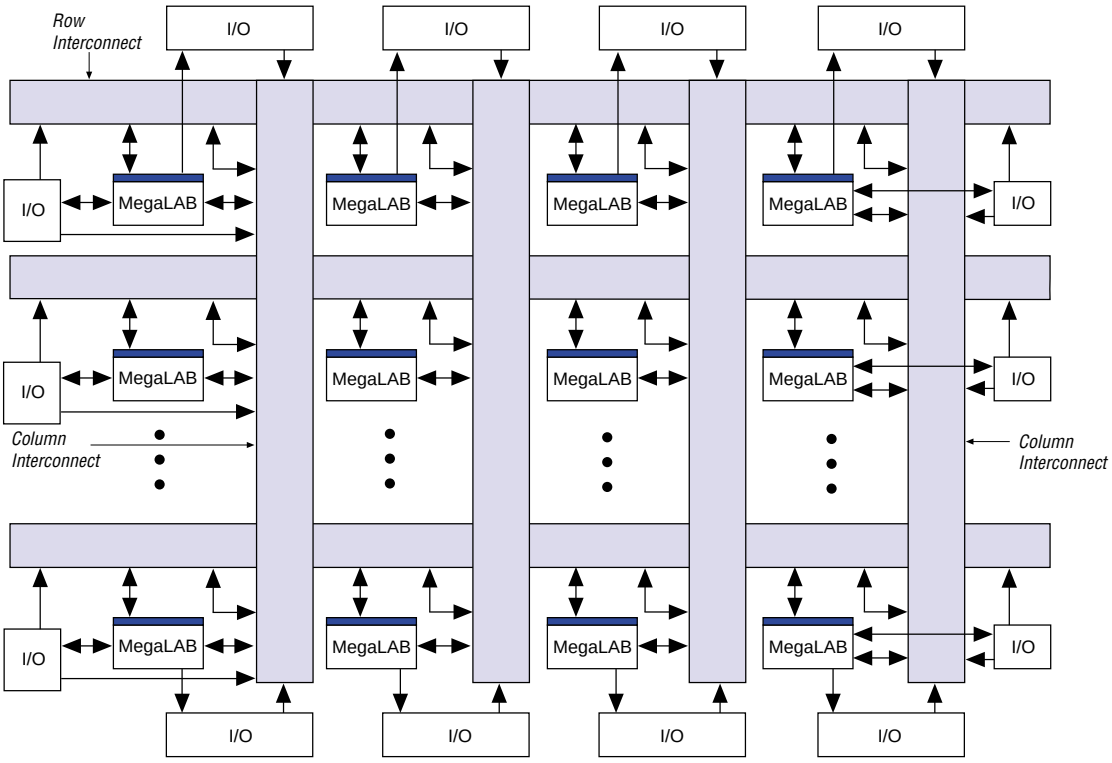
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX 20K Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

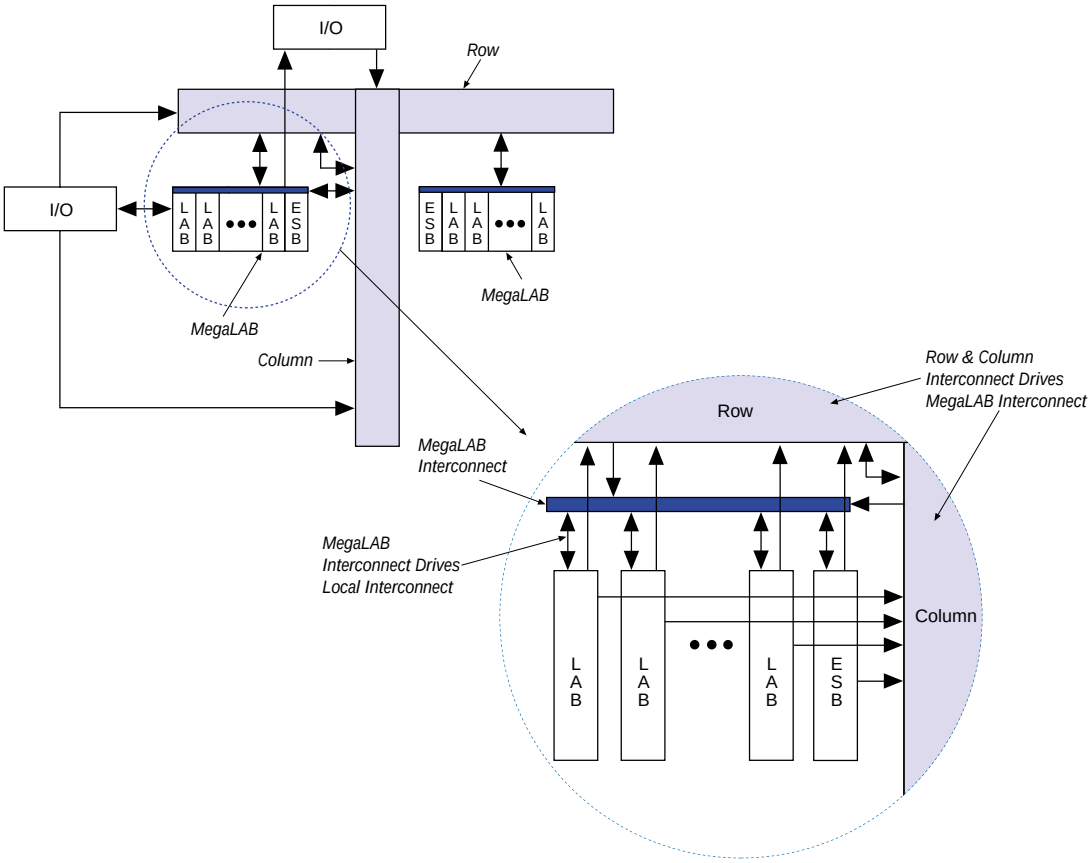
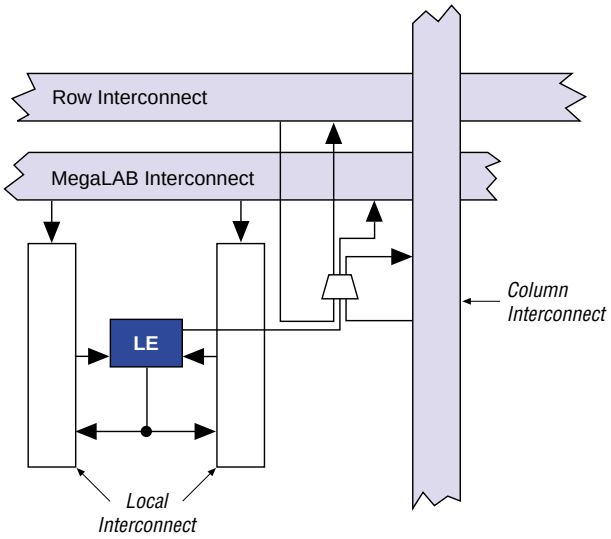


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the interconnect areas on the far left and far right of the MegaLAB. Figure 12 shows the FastRow interconnect.

Figure 12. APEX 20KE FastRow Interconnect

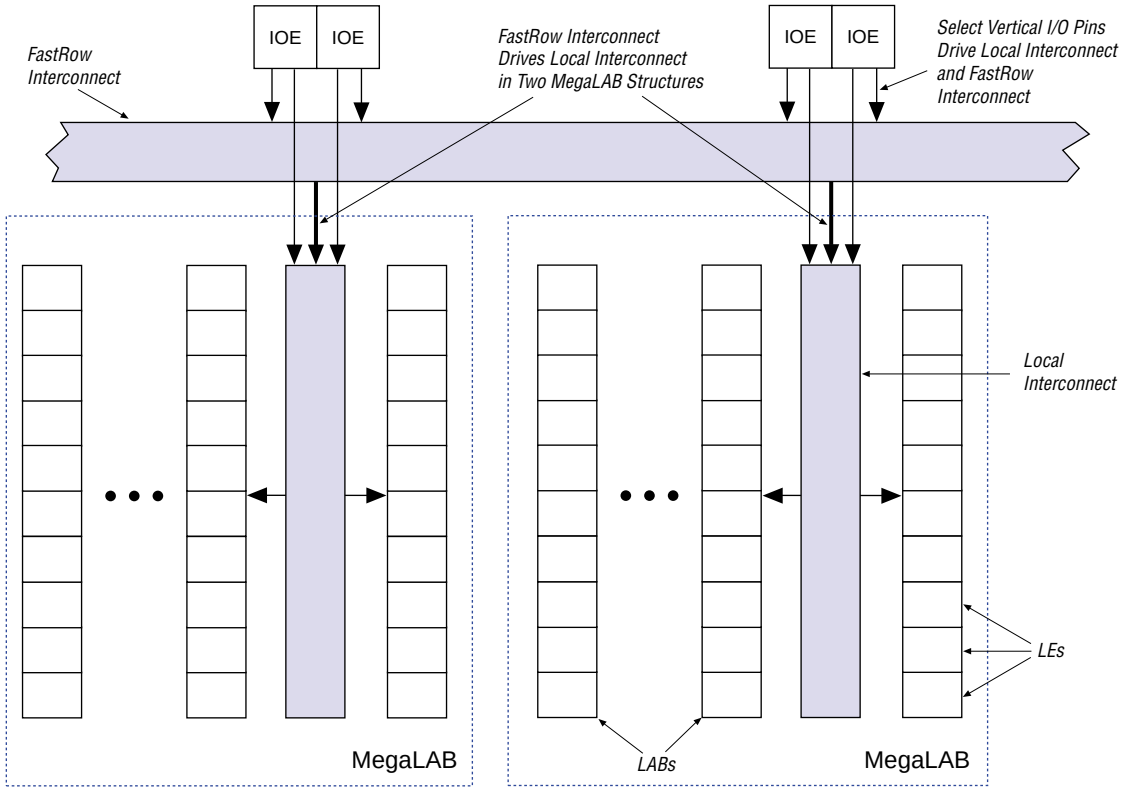


Table 8 summarizes how various elements of the APEX 20K architecture drive each other.

Table 8. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin					✓ *(1)*			✓	✓ *(1)*
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ *(1)*				

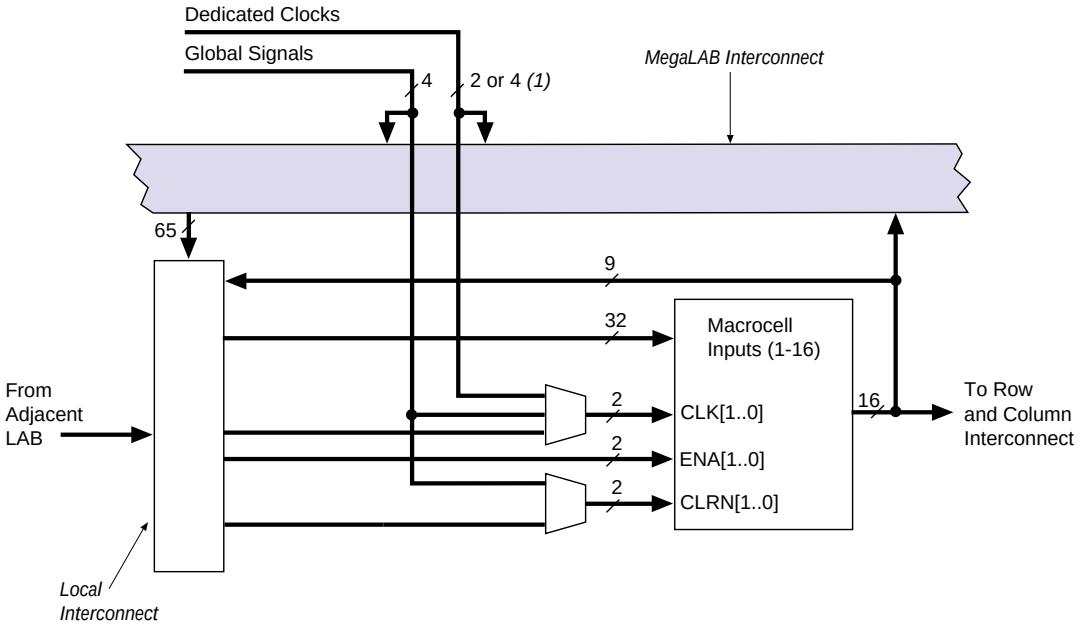
Note:
(1) This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

Figure 13. Product-Term Logic in ESB



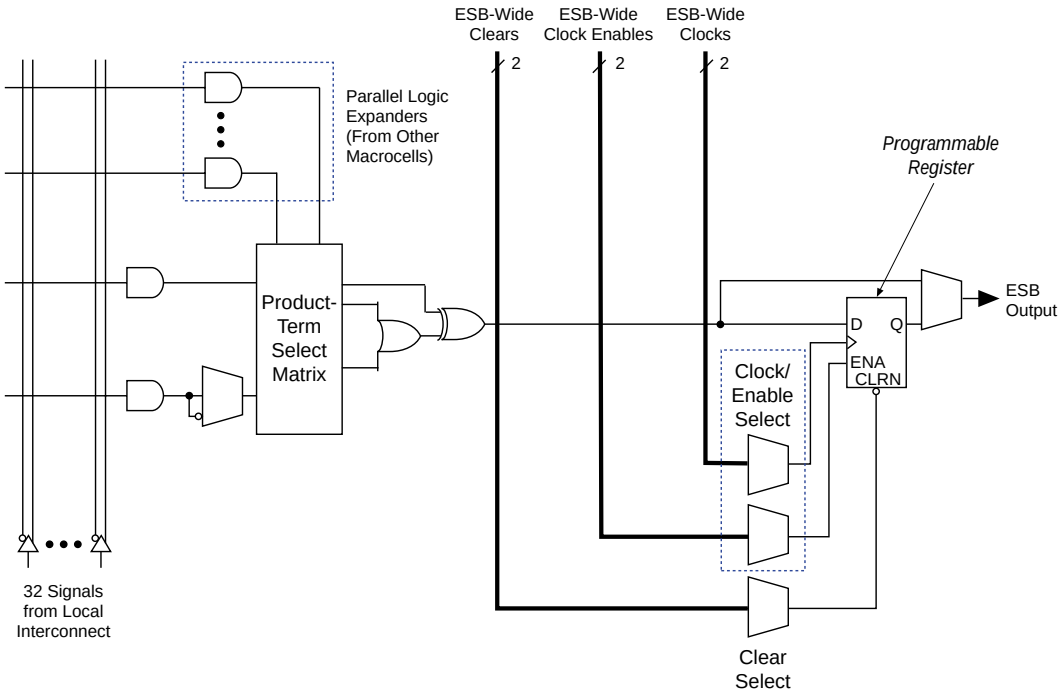
Note:
(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted: the Quartus software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

Figure 14. APEX 20K MacrocelI



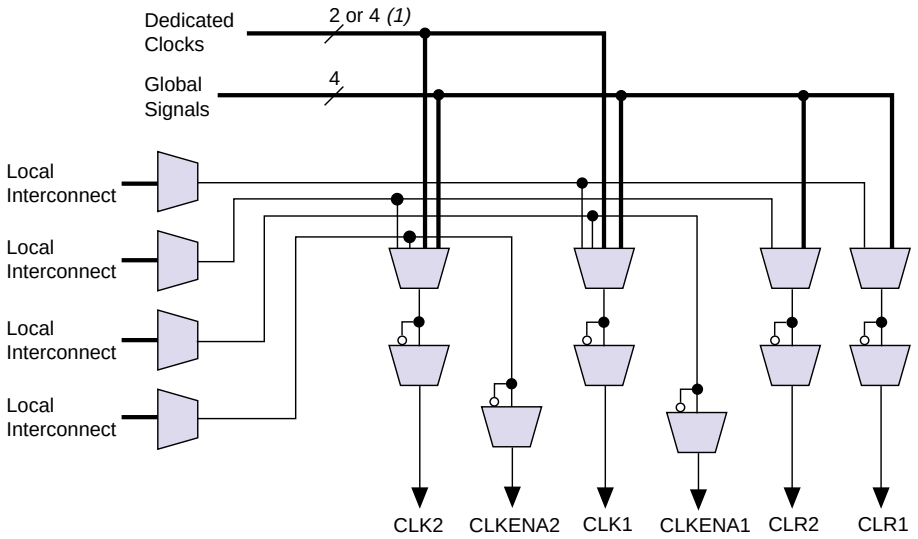
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



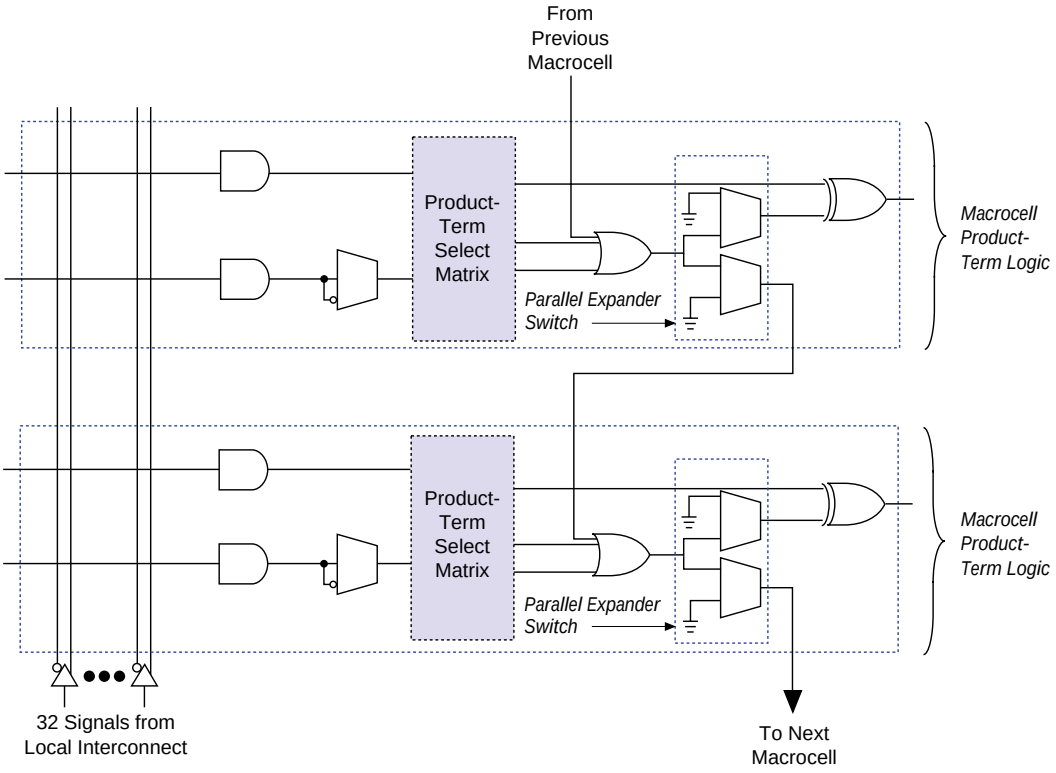
Note:
(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

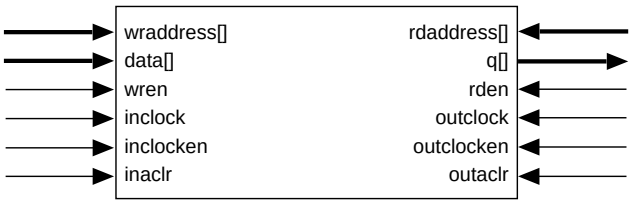
Figure 16. APEX 20K Parallel Expanders



Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

Figure 17. ESB Block Diagram



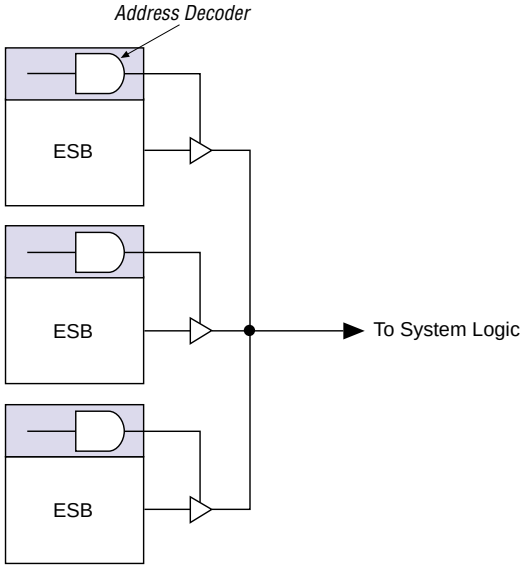
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

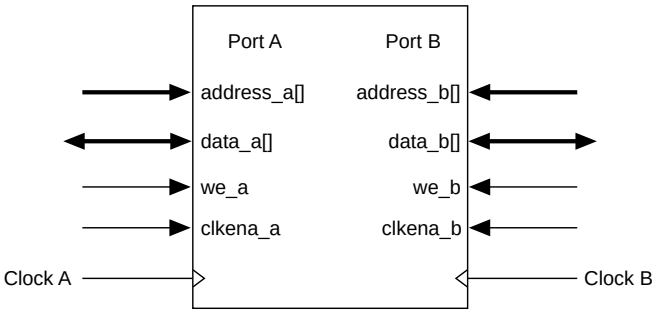
Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read / write clock mode and input / output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 19.

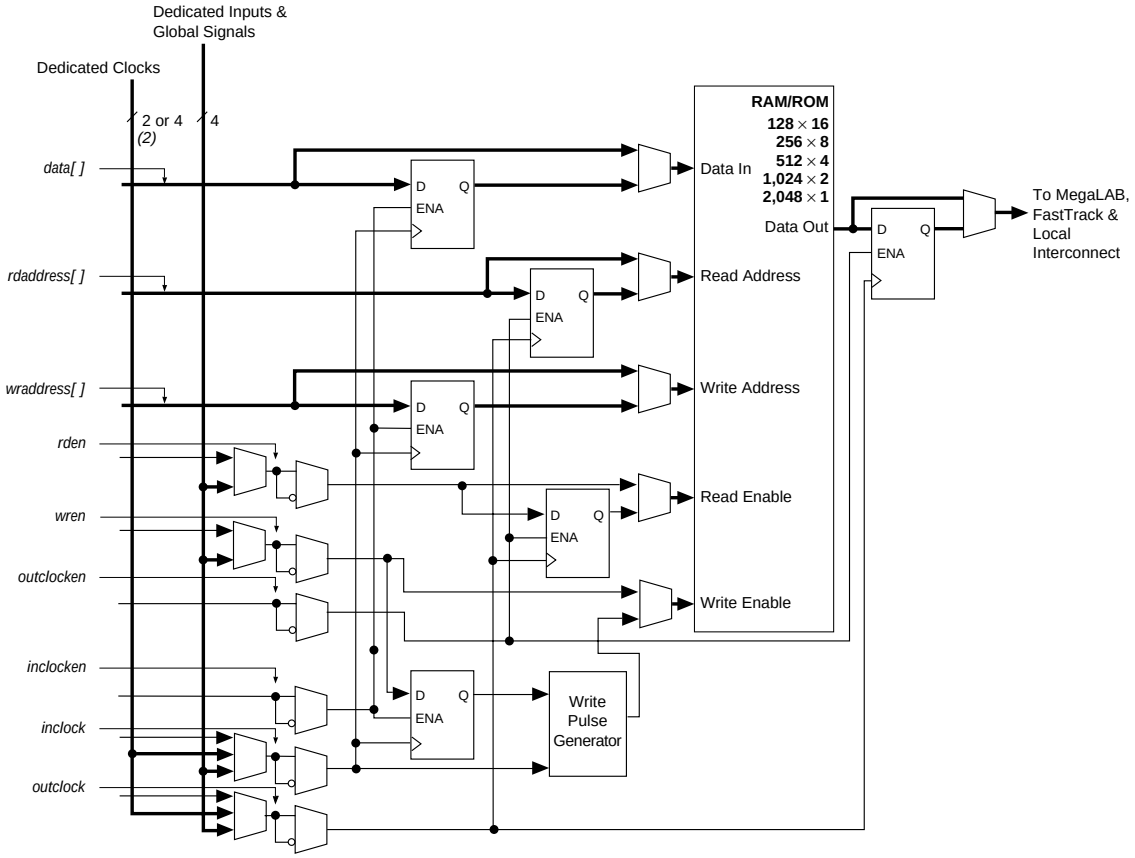
Figure 19. APEX 20K ESB Implementing Dual-Port RAM



Read/Write Clock Mode

The read / write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read / write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read / write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



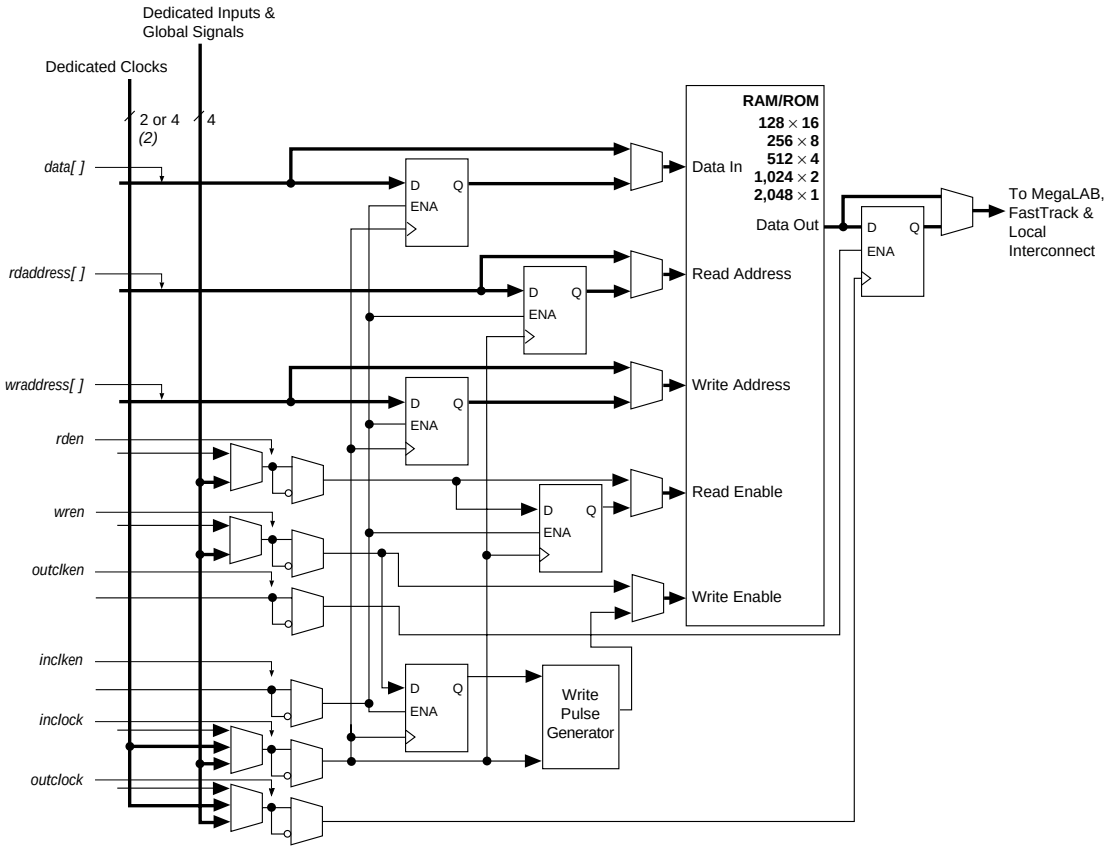
Notes:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode *Note (1)*



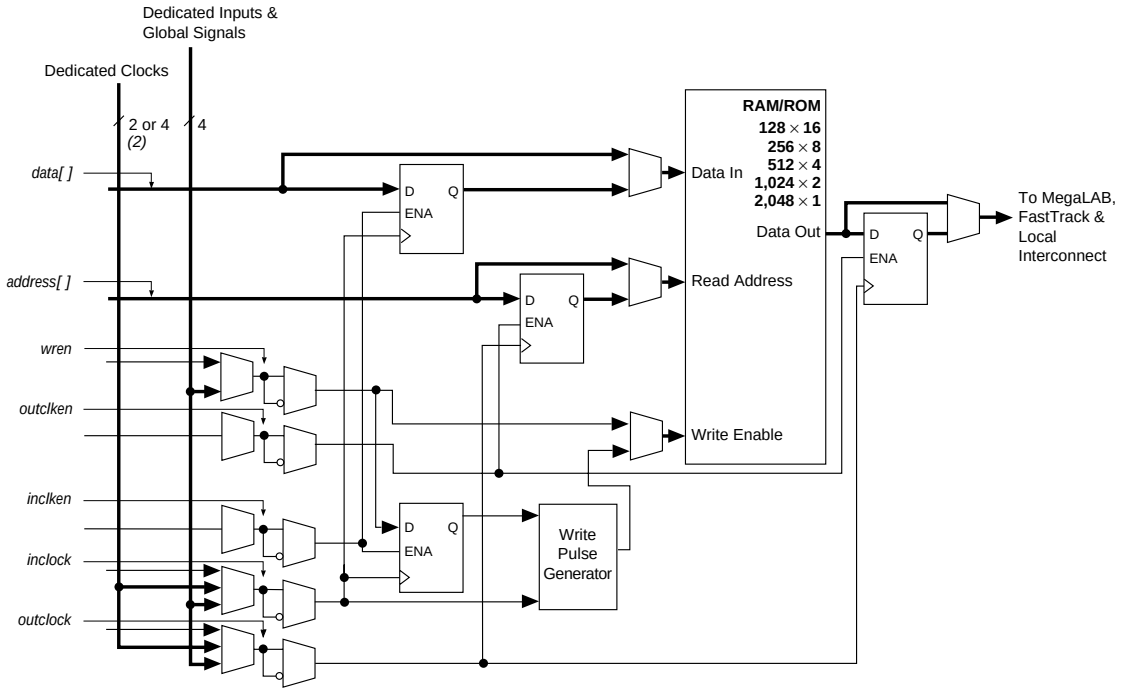
Notes:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



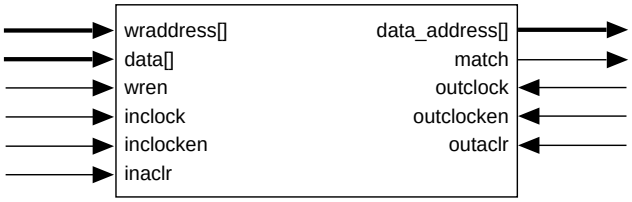
Notes:
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Figure 23. APEX 20KE CAM Block Diagram



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The don't-care bit can be used as a mask for CAM comparisons; any bit set to don't-care has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output, because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will not be correct. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

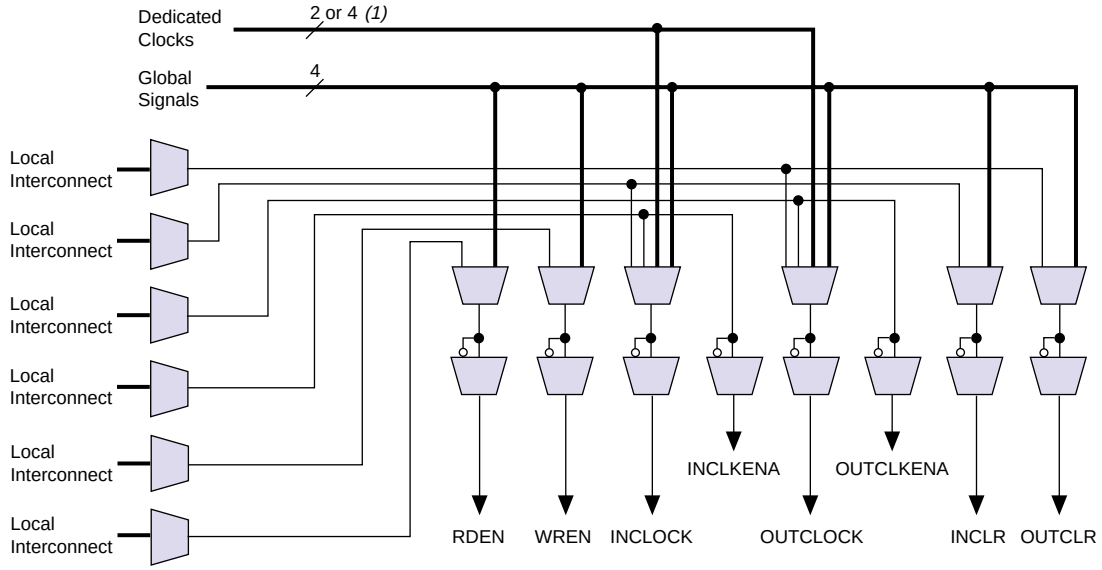
CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When don't-care bits are used, a third clock cycle is required.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



Note:
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20K I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 9 describes the APEX 20K programmable delays and their logic options in the Quartus software.

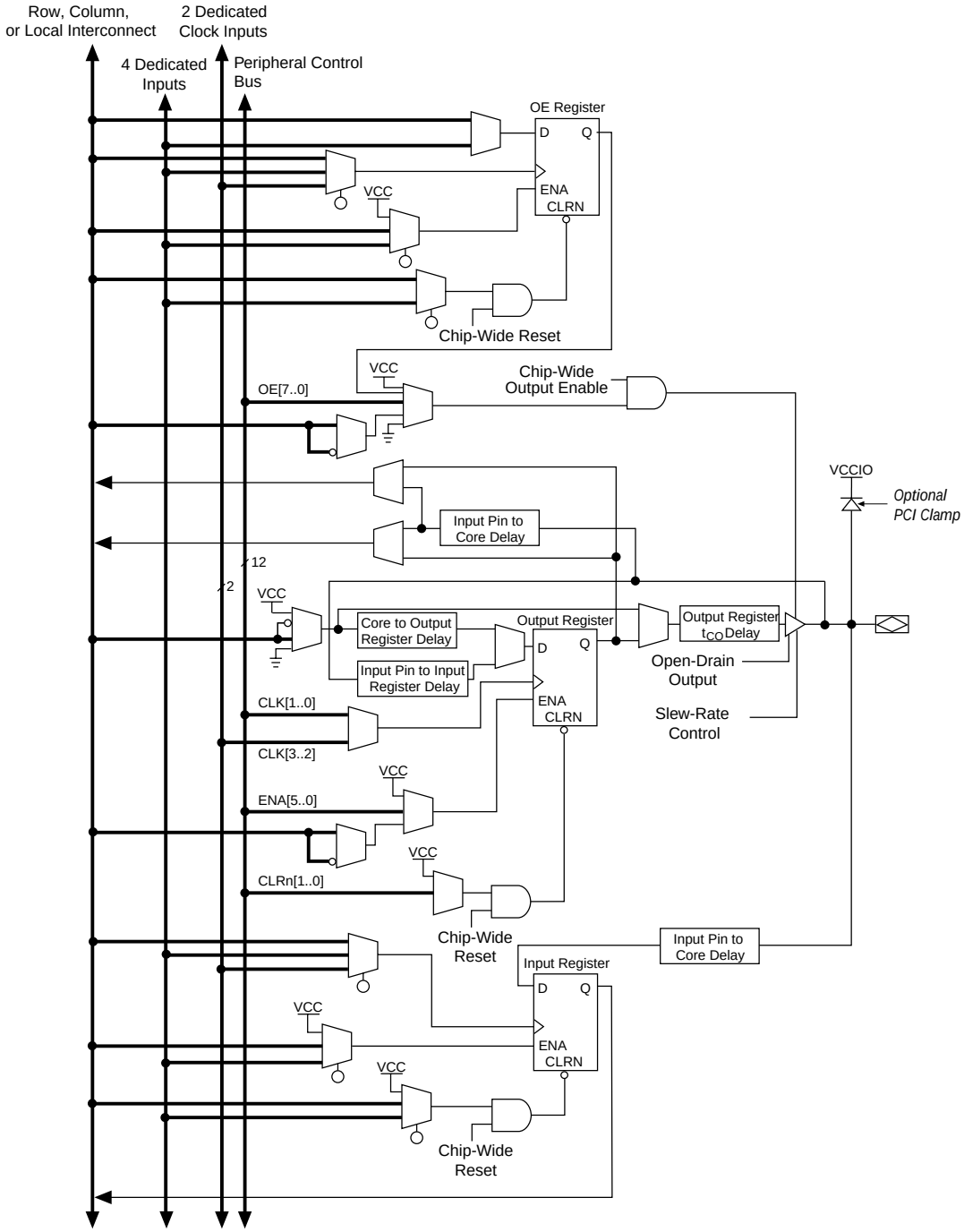
Table 9. APEX 20K Programmable Delay Chain

Programmable Delays	Quartus Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input register
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin

The Quartus Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power up high or low after configuration is complete. If it is programmed to power up low, an asynchronous clear can control the register. If it is programmed to power up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25. APEX 20K Bidirectional I/O Registers



APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus Compiler can set these delays automatically to minimize setup time while providing a zero hold time.

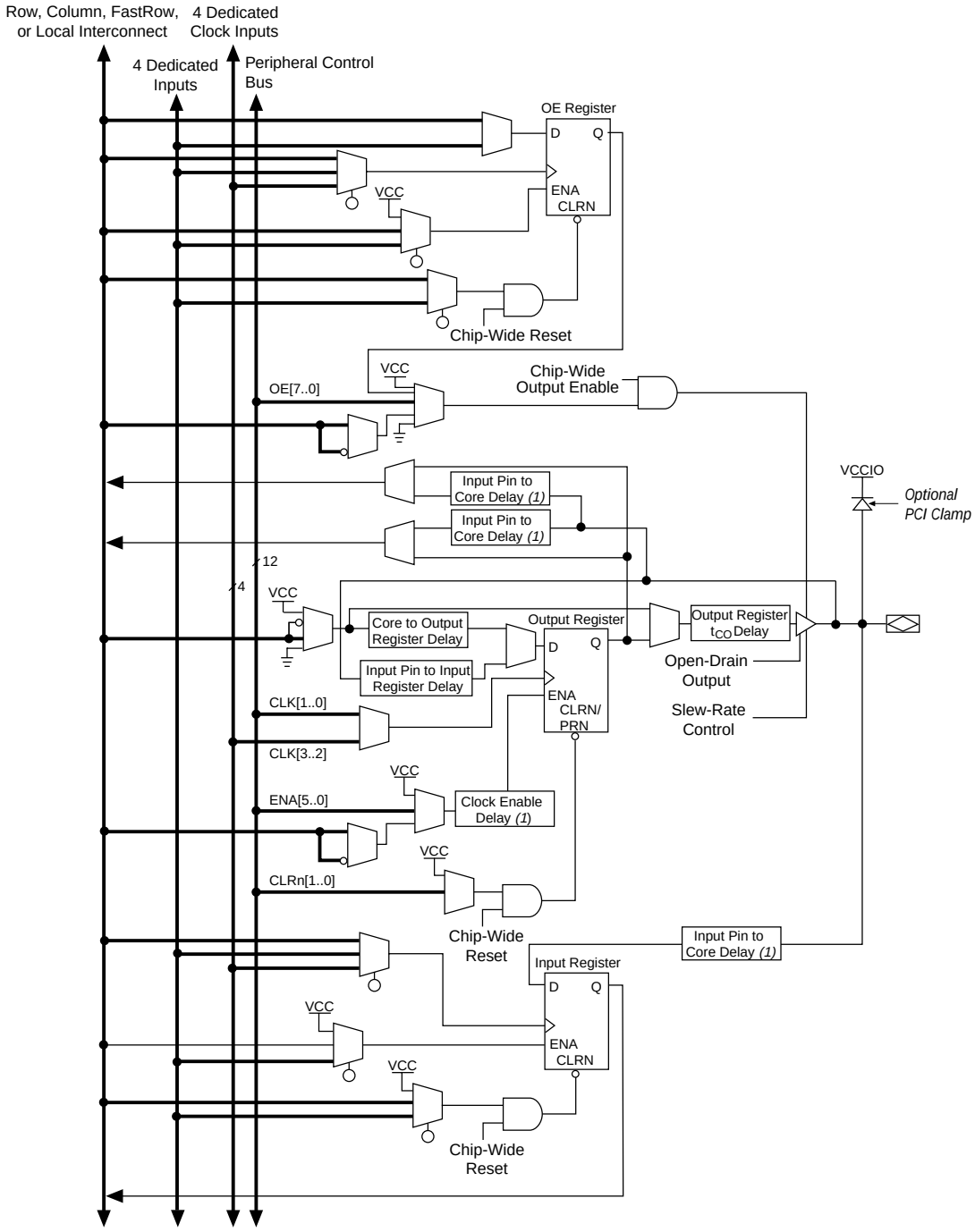
Table 10 describes the APEX 20KE programmable delays and their logic options in the Quartus software.

Table 10. APEX 20KE Programmable Delay Chains

Programmable Delays	Quartus Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power up high or low after configuration is complete. If it is programmed to power up low, an asynchronous clear can control the register. If it is programmed to power up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 26. APEX 20KE Bidirectional I/O Registers



Note:

(1) This programmable delay has four settings: off and three levels of delay.

Each IOE drives row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27 shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect

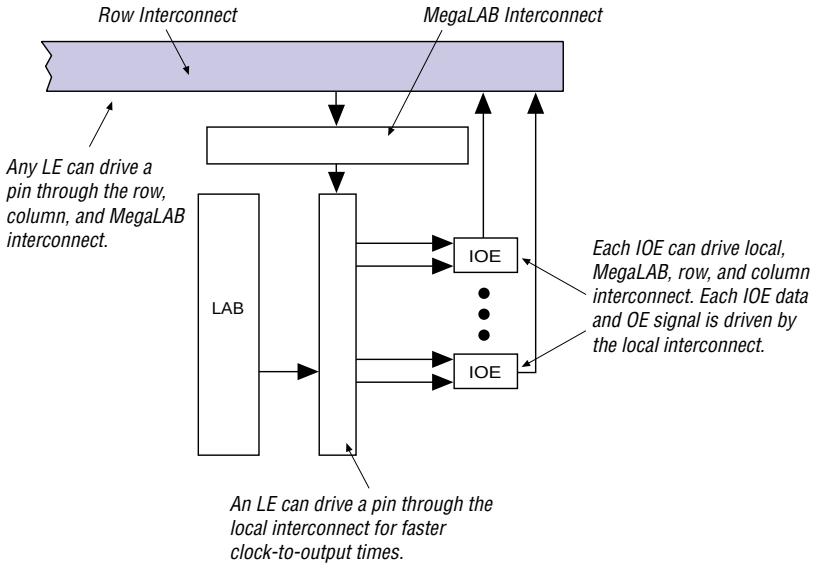
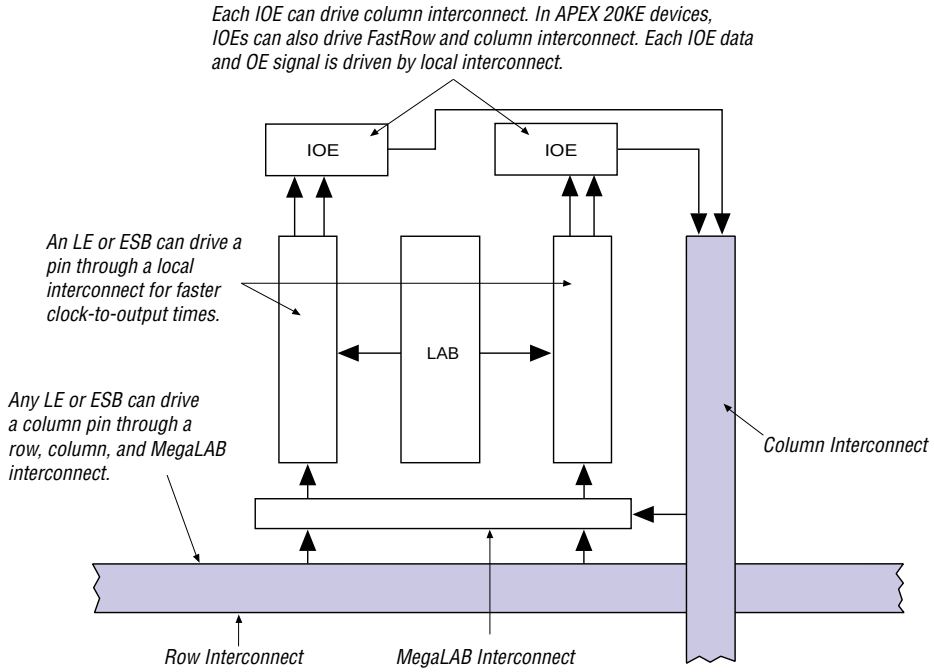


Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/Os

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/Os (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

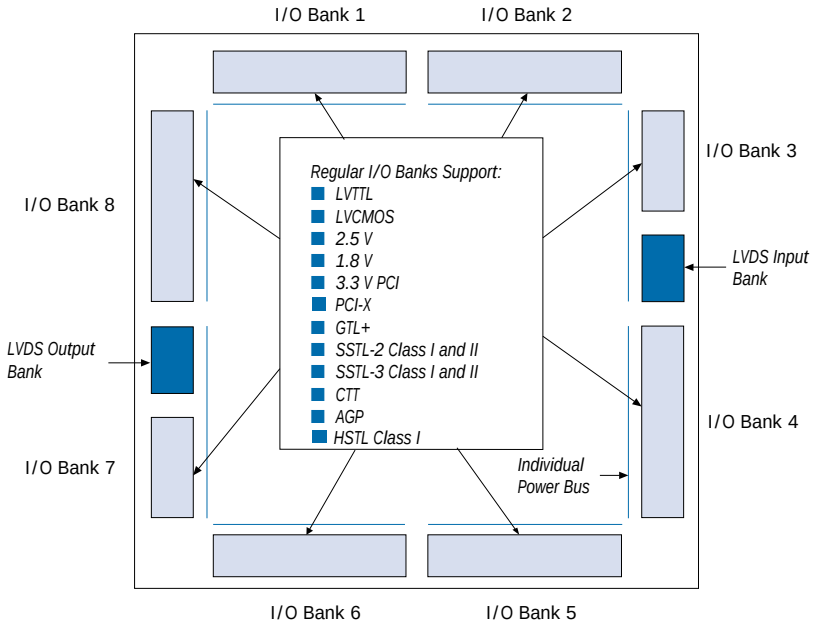
The APEX 20KE device contains eight I/O banks. The I/O banks support all standards except LVDS and LVPECLL. In addition, one bank supports LVDS and LVPELL inputs, and another bank supports LVDS and LVPELL outputs. The LVDS banks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level, so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K400E and larger devices support the LVDS interface for data pins up to 155 Mbit/channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for support up to 622 Mbit/channel.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for LVDS I/Os, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

Figure 29. APEX 20KE I/O Banks



Power Sequencing & Hot Socketing

Because APEX 20K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power planes may be powered in any order.

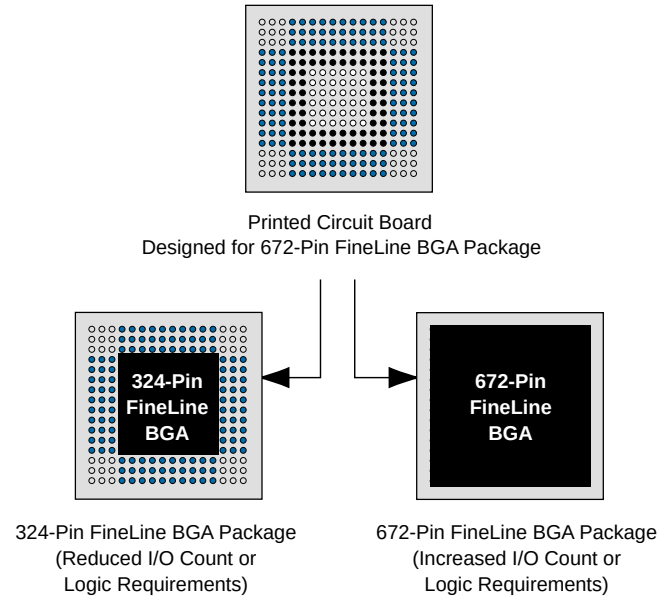
Signals can be driven into APEX 20K devices before and during power up without damaging the device. In addition, APEX 20K devices do not drive out during power up. Once operating conditions are reached and the device is configured, APEX 20K devices operate as specified by the user.

SameFrame Pin-Outs

APEX 20K devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EP20K60E device in a 324-pin FineLine BGA package to an EP20K1000E device in a 672-pin FineLine BGA package.

The Quartus software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Quartus software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 30).

Figure 30. SameFrame Pin-Out Example



MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V and 3.3-V tolerant. The devices, identified by a "V" suffix following the speed grade in the ordering code (e.g., EP20K400BC652-1V), are 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 11 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 11. 5.0-V Tolerant APEX 20K MultiVolt I/O Support

V_{CCIO} (V)	Input Signal			Output Signals		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1) (3)	✓		
3.3	✓	✓	✓ (1) (3)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.
(3) APEX 20K devices with a "V" suffix are 5.0-V tolerant.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes APEX 20KE MultiVolt I/O support.

Table 12. APEX 20KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signal			Output Signals			
	1.8	2.5	3.3	1.8	2.5	3.3	5.0
1.8	✓			✓			
2.5		✓	✓ (1)		✓		
3.3		✓	✓		✓ (2)	✓	✓

Notes to table:
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2) When VCCIO = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus software. External devices are not required to use these features.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 13 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 13. Multiplication Factor Combinations

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m, and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 77.76 MHz to support 622.08 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

50/50 Duty Cycle

The PLL output always goes through an internal division stage. Therefore, the PLL output always has a 50/50 duty cycle.

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The Lock signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 31 shows the incoming and generated clock specifications.

Figure 31. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

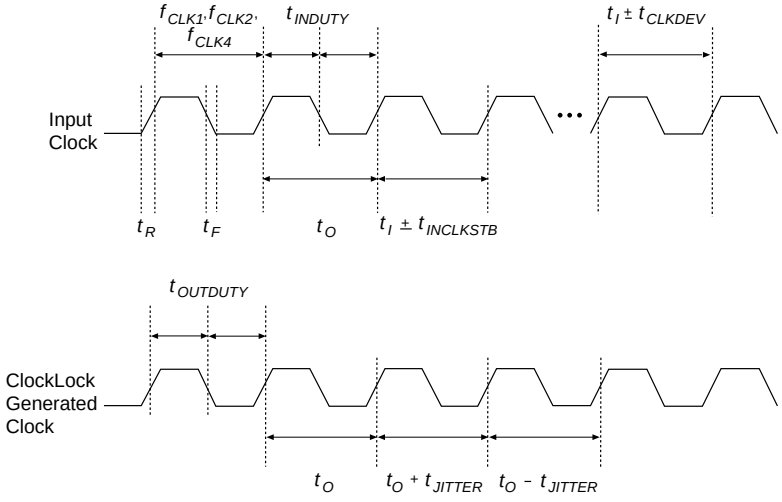


Table 14 summarizes the APEX 20K ClockLock and ClockBoost parameters for –1 speed grade devices.

Table 14. APEX 20K ClockLock & ClockBoost Parameters for –1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		200	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals two)		16		100	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)r)		10		48	MHz
f_{CLKDEV}	Input deviation from user specification in the Quartus software (ClockBoost clock multiplication factor equals 1) *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ < 100			250	ps
		$t_{INCLKSTB}$ < 50			200	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus software, designers must specify the input frequency. The Quartus software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation.

(2) 25,000 parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for –2 speed grade devices.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for –2 Speed Grade Devices (Part 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%

Table 15. APEX 20K ClockLock & ClockBoost Parameters for –2 Speed Grade Devices (Part 2 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)		10		34	MHz
f_{CLKDEV}	Input deviation from user specification in the Quartus software (ClockBoost clock multiplication factor equals one) *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ < 100			250	ps
		$t_{INCLKSTB}$ < 50			200	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus software, designers must specify the input frequency. The Quartus software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation.

Table 16 summarizes the ClockLock and ClockBoost parameters for APEX 20KE devices.

Table 16. APEX 20KE ClockLock & ClockBoost Parameters (Part 1 of 2) *Notes (1), (2)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{IN1}	Input clock frequency		1.5		160	MHz
f_{clock0}	Output clock frequency for clock0 output of the PLL		1.5		200	MHz
f_{clock1}	Output clock frequency for clock1 output of the PLL		20		200	MHz

Table 16. APEX 20KE ClockLock & ClockBoost Parameters (Part 2 of 2) Notes (1), (2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (2)				10	ms
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (3)	$t_{INCLKSTB}$ < 100			250	ps
		$t_{INCLKSTB}$ < 50			200	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		50		50	%

Notes:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The PLL VCO frequency range is 200 MHz f_{VCO} < 400 MHz.
(3) The maximum output frequency for the optional external clock output pins, `CLKLK_OUT1p` and `CLKLK_OUT2p`, is 150 MHz.

SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 17.

Table 17. APEX 20K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster or ByteBlasterMV download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 18 and 20 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 18. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	*(1)*
EP20K60E	654
EP20K100	786
EP20K100E	774
EP20K160E	1,176
EP20K200	1,164
EP20K200E	1,188
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,866
EP20K1000E	2,190
EP20K1500E	2,502

Note:
(1) Contact Altera Applications for up-to-date information on this device.

Table 19. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K30E	*(3)*	*(3)*	000 0110 1110 *(3)*	*(1)*
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1
EP20K1500E	0000	1001 0101 0000 0000	000 0110 1110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.
(3) Contact Altera Applications for up-to-date information on this device.

Figure 32 shows the timing requirements for the JTAG signals.

Figure 32. APEX 20K JTAG Waveforms

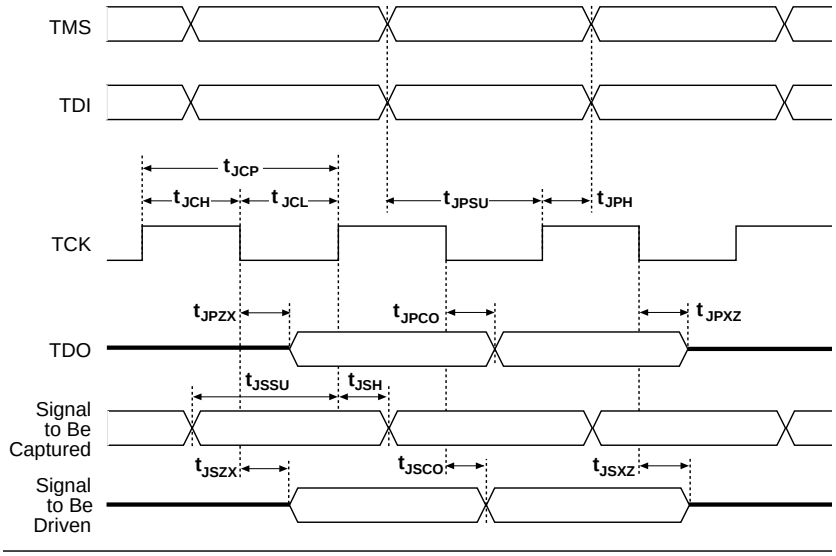


Table 20 shows the JTAG timing parameters and values for APEX 20K devices.

Table 20. APEX 20K JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information, see the following documents:

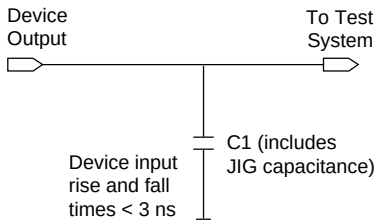
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 33. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 33. APEX 20K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Operating Conditions

Tables 21 through 24 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 21. APEX 20K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 22. APEX 20K Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0°	85°	C
		For industrial use	–40°	100°	C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 23. APEX 20K Device DC Operating Conditions (Part 1 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, $0.5 \times V_{CCIO}$ *(8)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, $0.3 \times V_{CCIO}$ *(8)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V

Table 23. APEX 20K Device DC Operating Conditions (Part 2 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(11)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(11)*	30		80	kΩ

Table 24. APEX 20K Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25 °C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20K device recommended operating conditions, shown in Table 22 on page 58.
(8) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 34 on page 66.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Tables 25 through 28 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V tolerant APEX 20K devices. These devices are identified by a "V" suffix following the speed grade in the ordering code (e.g., EP20K400BC652-1V).

Table 25. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	-0.5	3.6	V
V_{CCIO}			-0.5	4.6	V
V_I	DC input voltage		-2.0	5.75	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	° C
T_{AMB}	Ambient temperature	Under bias	-65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 26. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*,*(4)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2)*, *(5)*	– 0.5	5.75	V
V_O	Output voltage		0	VCCIO	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 27. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, 0.5 × V_{CCIO} *(8)*		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(8)*	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V*(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V*(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V

Table 27. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, –2, –3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(11)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(11)*	30		80	kΩ

Table 28. APEX 20K 5.0-V Tolerant Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to -0.5 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25 °C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 or 3.3 V.
(7) These values are specified in the APEX 20KE device recommended operating conditions, shown in Table 26 on page 63.
(8) The APEX 20KE input buffers are compatible with 1.8-V, and 3.3-V (LVTTL and LVCMOS). Additionally, the input buffers are 3.3-V PCI compliant. When V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 34 on page 65.

(9) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Tables 29 through 32 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 29. APEX 20KE Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 30. APEX 20KE Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 31. APEX 20KE Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V_{CCIO} *(8)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(8)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, –1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, –2, –3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(11)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(11)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(11)*	60		150	kΩ

☞ For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

Table 32. APEX 20K Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20K device recommended operating conditions, shown in Table 30 on page 63.
(8) The APEX 20K input buffers are compatible with 1.8 -V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Figure 34 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance on APEX 20K devices. For information on this relationship on APEX 20KE devices, contact Altera Applications.

Figure 34. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

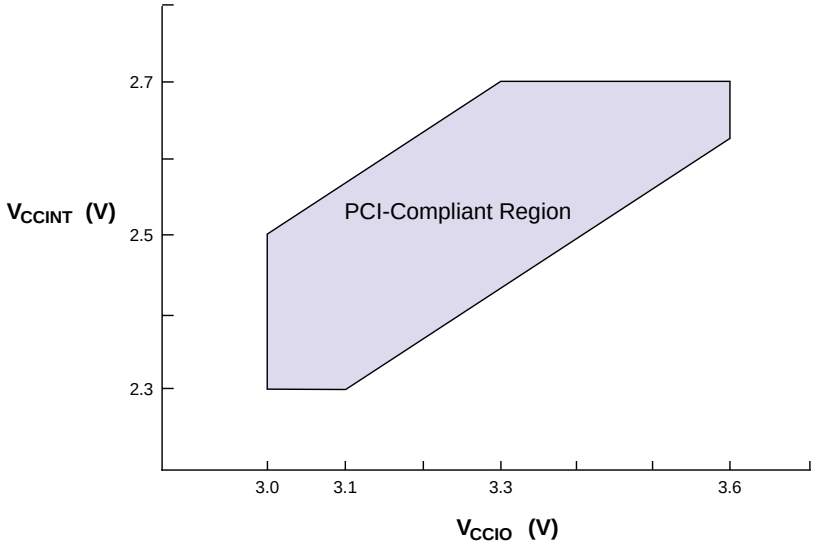
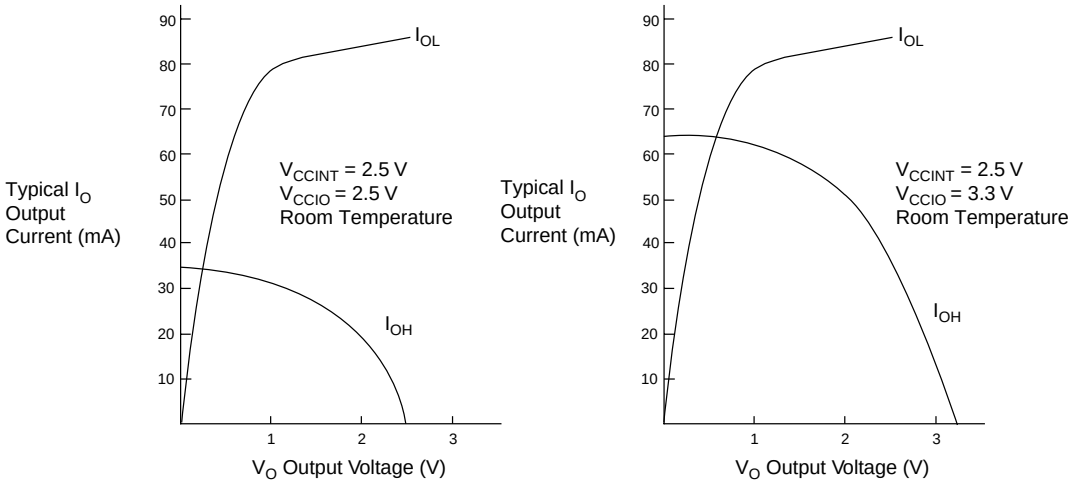


Figure 35 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification***, ***Revision 2.2*** (when VCCIO pins are connected to 3.3 V). For output drive characteristics of APEX 20KE devices, contact Altera Applications.

Figure 35. Output Drive Characteristics of APEX 20K Device

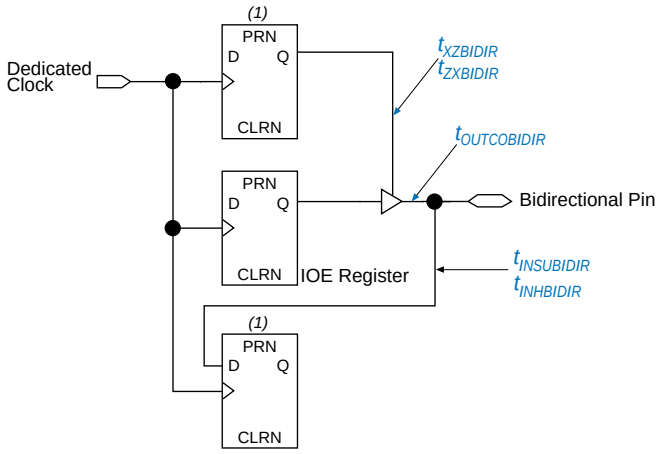


Timing Model

The continuous, high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 36 shows the timing model for bidirectional I/O pin timing.

Figure 36. Synchronous Bidirectional Pin External Timing



Note:
(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Tables 33 and 34 describe APEX 20K external timing parameters.

Table 33. APEX 20K External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 34. External Bidirectional Timing Parameters *Note (1)* ***(Part 1 of 2)***

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	

Table 34. External Bidirectional Timing Parameters Note (1) (Part 2 of 2)		
Symbol	**Parameter**	**Condition**
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 35 pF

Note to tables:
(1) These timing parameters are sample-tested only.

Figure 37 shows the f_{MAX} timing model for APEX 20K and APEX 20KE devices.

Figure 37. f_{MAX} Timing Model

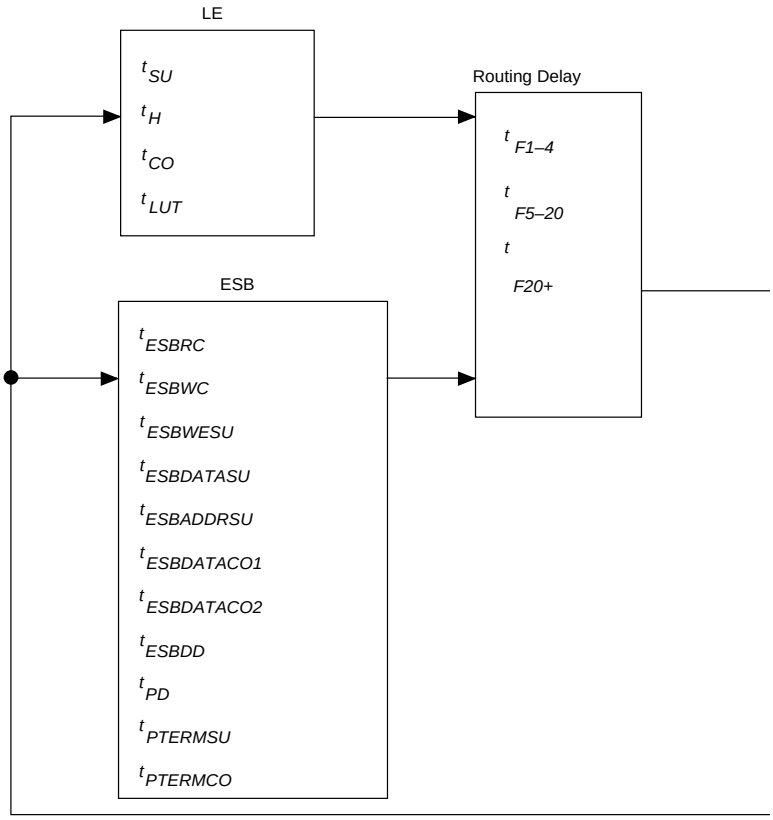


Table 35 describes the f_{MAX} timing parameters shown in Figure 37.

Table 35. APEX 20K & APEX 20KE f_{MAX} Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in
t_{ESBRC}	ESB Asynchronous read cycle time
t_{ESBWC}	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBADDRSU}$	ESAB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay
t_{F1-4}	Fanout delay using Local Interconnect
t_{F5-20}	Fanout delay using MegaLab Interconnect
t_{F20+}	Fanout delay using FastTrack Interconnect
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear Pulse Width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 36 through 40 show the $\mathbf{f_{MAX}}$ timing parameters for EP20K100, EP20K200, EP20K400, EP20K400E, and EP20K600E devices.

Table 36. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.5		0.6		0.8	
t_{H}	0.7		0.8		1.0	
t_{CO}		0.3		0.4		0.5
t_{LUT}		0.8		0.9		1.3
t_{ESBRC}		3.8		4.5		5.3
t_{ESBWC}		1.9		2.2		2.6
$t_{ESBWESU}$	1.2		1.4		1.7	
$t_{ESBDATASU}$	1.2		1.5		1.7	
$t_{ESBADDRSU}$	1.1		1.3		1.6	
$t_{ESBDATACO1}$		0.9		1.1		1.3
$t_{ESBDATACO2}$		6.2		7.3		8.7
t_{ESBDD}		3.8		4.6		5.4
t_{PD}		2.5		3.0		3.6
$t_{PTERMSU}$	2.3		2.8		3.3	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.6		0.8		0.8
t_{F5-20}		1.0		1.6		1.9
t_{F20+}		2.4		3.2		3.8
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.4		0.4		0.5	
t_{PREP}	0.4		0.4		0.5	
t_{ESBCH}	2.1		2.5		3.0	
t_{ESBCL}	2.1		2.5		3.0	
t_{ESBWP}	1.7		2.0		2.4	
t_{ESBRP}	1.1		1.3		1.6	

Table 37. EP20K200 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.5		0.6		0.8	
t_{H}	0.7		0.8		1.0	
t_{CO}		0.3		0.4		0.5
t_{LUT}		0.8		0.9		1.3
t_{ESBRC}		3.8		4.5		5.3
t_{ESBWC}		1.9		2.2		2.6
$t_{ESBWESU}$	1.2		1.4		1.7	
$t_{ESBDATASU}$	1.2		1.5		1.7	
$t_{ESBADDRSU}$	1.1		1.3		1.6	
$t_{ESBDATACO1}$		0.9		1.1		1.3
$t_{ESBDATACO2}$		6.4		7.5		8.9
t_{ESBDD}		3.8		4.6		5.4
t_{PD}		2.5		3.0		3.6
$t_{PTERMSU}$	2.3		2.8		3.3	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.6		0.8		0.8
t_{F5-20}		1.1		1.6		1.9
t_{F20+}		2.4		3.2		3.8
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.4		0.4		0.5	
t_{PREP}	0.4		0.4		0.5	
t_{ESBCH}	2.1		2.5		3.0	
t_{ESBCL}	2.1		2.5		3.0	
t_{ESBWP}	1.7		2.0		2.4	
t_{ESBRP}	1.1		1.3		1.6	

Table 38. EP20K400 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.1		0.3		0.6	
t_{H}	0.5		0.8		0.9	
t_{CO}		0.1		0.4		0.6
t_{LUT}		0.8		1.0		1.1
t_{ESBRC}		2.3		2.8		3.3
t_{ESBWC}		2.9		3.5		4.1
$t_{ESBWESU}$	3.2		3.8		4.5	
$t_{ESBDATASU}$	2.2		2.6		3.0	
$t_{ESBADDRSU}$	0.4		0.4		0.5	
$t_{ESBDATACO1}$		0.3		0.3		0.4
$t_{ESBDATACO2}$		6.3		7.7		9.0
t_{ESBDD}		5.7		6.9		8.1
t_{WDSU}		1.3		1.4		1.6
t_{PD}		2.5		3.1		3.6
$t_{PTERMSU}$	1.7		2.0		2.4	
$t_{PTERMCO}$		0.1		0.3		0.4
t_{F1-4}		0.5		0.7		0.8
t_{F5-20}		1.2		1.4		1.9
t_{F20+}		5.9		6.6		7.4
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.5		0.6		0.8	
t_{PREP}	0.5		0.6		0.8	
t_{ESBCH}	2.0		2.5		3.0	
t_{ESBCL}	2.0		2.5		3.0	
t_{ESBWP}	1.5		1.9		2.2	
t_{ESBRP}	1.0		1.2		1.4	

Table 39. EP20K400E f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.5		0.6		0.8	
t_{H}	0.7		0.8		1.0	
t_{CO}		0.3		0.4		0.5
t_{LUT}		0.8		0.9		1.1
t_{ESBRC}		3.8		4.5		5.3
t_{ESBWC}		1.9		2.2		2.6
$t_{ESBWESU}$	1.2		1.4		1.7	
$t_{ESBDATASU}$	1.2		1.5		1.7	
$t_{ESBADDRSU}$	1.1		1.3		1.6	
$t_{ESBDATACO1}$		0.9		1.1		1.3
$t_{ESBDATACO2}$		5.6		6.6		7.9
t_{ESBDD}		3.8		4.6		5.4
t_{PD}		2.5		3.0		3.6
$t_{PTERMSU}$	2.3		2.8		3.3	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.5		0.6		0.6
t_{F5-20}		0.8		1.1		1.6
t_{F20+}		3.5		4.3		5.3
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.4		0.4		0.5	
t_{PREP}	0.4		0.4		0.5	
t_{ESBCH}	2.1		2.5		3.0	
t_{ESBCL}	2.1		2.5		3.0	
t_{ESBWP}	1.7		2.0		2.4	
t_{ESBRP}	1.1		1.3		1.6	

Table 40. EP20K600E f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.5		0.6		0.8	
t_{H}	0.7		0.8		1.0	
t_{CO}		0.3		0.4		0.5
t_{LUT}		0.8		0.9		1.1
t_{ESBRC}		3.8		4.5		5.3
t_{ESBWC}		1.9		2.2		2.6
$t_{ESBWESU}$	1.2		1.4		1.7	
$t_{ESBDATASU}$	1.2		1.5		1.7	
$t_{ESBADDRSU}$	1.1		1.3		1.6	
$t_{ESBDATACO1}$		0.9		1.1		1.3
$t_{ESBDATACO2}$		5.6		6.6		7.9
t_{ESBDD}		3.8		4.6		5.4
t_{PD}		2.5		3.0		3.6
$t_{PTERMSU}$	2.3		2.8		3.3	
$t_{PTERMCO}$		0.9		1.1		1.3
$t_{F1–4}$		0.5		0.5		0.5
t_{F5-20}		0.8		1.1		1.6
t_{F20+}		3.5		4.3		5.3
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.4		0.4		0.5	
t_{PREP}	0.4		0.4		0.5	
t_{ESBCH}	2.1		2.5		3.0	
t_{ESBCL}	2.1		2.5		3.0	
t_{ESBWP}	1.7		2.0		2.4	
t_{ESBRP}	1.1		1.3		1.6	

Tables 41 through 50 show the I/O timing parameter values for APEX 20K devices.

Table 41. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.3		1.4		1.8		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t_{INSU} (2)	1.1		1.2		1.6		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	0.5	4.8	ns
t_{PCISU}	3.0		3.0		3.0		ns
t_{PCIH}	0.0		0.0		0.0		ns
t_{PCICO}	2.0	6.0	2.0	6.0	2.0	6.0	ns

Table 42. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.2		1.4		1.8		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.0		1.2		1.6		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	0.5	4.8	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		5.9	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		5.9	ns

Table 43. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.8		1.4		1.9		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t_{INSU} (2)	1.1		1.2		1.7		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	0.5	4.8	ns
t_{PCISU}	3.0		3.0		3.0		ns
t_{PCIH}	0.0		0.0		0.0		ns
t_{PCICO}	2.0	6.0	2.0	6.0	2.0	6.0	ns

Table 44. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.3		1.4		1.8		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.0		1.2		1.6		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	0.5	4.8	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		5.9	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		5.9	ns

Table 45. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	0.6		1.2		1.9		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
t_{INSU} (2)	0.4		1.0		1.7		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	3.1	0.5	4.1	0.5	5.1	ns
t_{PCISU}	3.0		3.0		3.0		ns
t_{PCIH}	0.0		0.0		0.0		ns
t_{PCICO}	2.0	6.0	2.0	6.0	2.0	6.0	ns

Table 46. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	0.7		1.2		1.9		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{XZBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{ZXBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{INSUBIDIR}$ (2)	0.5		1.0		1.7		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.1	0.5	4.1	0.5	5.1	ns
$t_{XZBIDIR}$ (2)		6.2		7.6		8.8	ns
$t_{ZXBIDIR}$ (2)		6.2		7.6		8.8	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.
(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 47. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	0.6		1.0		1.6		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.1	2.0	5.1	2.0	5.9	ns
t_{INSU} (2)	0.4		0.8		1.4		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	2.3	0.5	3.3	0.5	4.1	ns
t_{PCISU}	3.0		3.0		3.0		ns
t_{PCIH}	0.0		0.0		0.0		ns
t_{PCICO}	2.0	6.0	2.0	6.0	2.0	6.0	ns

Table 48. EP20K400E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	0.7		1.0		1.6		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	6.3	2.0	7.5	2.0	8.9	ns
$t_{XZBIDIR}$ (1)		4.0		4.7		5.8	ns
$t_{ZXBIDIR}$ (1)		4.0		4.7		5.8	ns
$t_{INSUBIDIR}$ (2)	0.5		0.8		1.4		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	2.0	4.1	2.0	5.1	2.0	5.9	ns
$t_{XZBIDIR}$ (2)		3.4		4.0		4.9	ns
$t_{ZXBIDIR}$ (2)		3.4		4.0		4.9	ns

Table 49. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	0.6		1.0		1.6		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.1	2.0	5.1	2.0	5.9	ns
t_{INSU} (2)	0.4		0.8		1.4		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	2.3	0.5	3.3	0.5	4.1	ns
t_{PCISU}	3.0		3.0		3.0		ns
t_{PCIH}	0.0		0.0		0.0		ns
t_{PCICO}	2.0	6.0	2.0	6.0	2.0	6.0	ns

Table 50. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	0.7		1.0		1.6		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	6.3	2.0	7.5	2.0	8.9	ns
$t_{XZBIDIR}$ (1)		4.0		4.7		5.8	ns
$t_{ZXBIDIR}$ (1)		4.0		4.7		5.8	ns
$t_{INSUBIDIR}$ (2)	0.5		0.8		1.4		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	2.0	4.1	2.0	5.1	2.0	5.9	ns
$t_{XZBIDIR}$ (2)		3.4		4.0		4.9	ns
$t_{ZXBIDIR}$ (2)		3.4		4.0		4.9	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits. ClockShift was not used in this measurement. ClockShift can be used to adjust the setup and clock-to-output times to achieve the desired results.

Tables 51 and 52 show selectable input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 51. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0		0.0		0.0	ns
LVTTL		0.0		0.0		0.0	ns
2.5 V		0.1		0.2		0.2	ns
1.8 V		0.5		0.6		0.8	ns
PCI		0.4		0.5		0.7	ns
GTL+		–0.3		–0.4		–0.5	ns
SSTL-3 Class I		–0.4		–0.5		–0.6	ns
SSTL-3 Class II		–0.4		–0.5		–0.6	ns
SSTL-2 Class I		–0.3		–0.3		–0.4	ns
SSTL-2 Class II		–0.3		–0.3		–0.4	ns
LVDS		–0.2		–0.3		–0.4	ns
CTT		–0.3		–0.3		–0.4	ns
AGP		0.0		0.1		0.1	ns

Table 52. Selectable I/O Standard Output Delays (Part 1 of 2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0		0.0		0.0	ns
LVTTL		0.0		0.0		0.0	ns
2.5 V		0.5		0.6		0.7	ns
1.8 V		1.7		2.2		2.7	ns
PCI		–0.2		–0.3		–0.4	ns
GTL+		–0.4		–0.5		–0.6	ns
SSTL-3 Class I		–0.1		–0.2		–0.2	ns
SSTL-3 Class II		–0.6		–0.8		–1.0	ns
SSTL-2 Class I		0.0		0.0		0.0	ns
SSTL-2 Class II		–0.4		–0.5		–0.6	ns
LVDS		–0.8		–1.0		–1.2	ns
CTT		–0.2		–0.3		–0.4	ns

Table 52. Selectable I/O Standard Output Delays (Part 2 of 2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
AGP		–0.4		–0.5		–0.7	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/Os are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 53), chosen on the basis of the target application. An EPC2 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When an EPC2 configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 53. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC2 configuration device
Passive serial (PS)	ByteBlasterMV or MasterBlaster download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

Table 54 shows the pin names and numbers for EP20K100 devices in 144-pin TQFP, 208-pin PQFP, 240-pin PQFP, and 324-pin FineLine BGA packages.

Table 54. EP20K100 Device Pin-Outs (Part 1 of 2) *Note (1)*

Pin Name	144-Pin TQFP	208-Pin PQFP (2)	240-Pin PQFP (3)	324-Pin FineLine BGA (1)	356-Pin BGA EP20K100 (1)
MSEL0 (4)	18	25	29	J17	P1
MSEL1 (4)	19	26	30	J16	P2
NSTATUS (4)	57	82	92	U9	AF15
NCONFIG (4)	22	29	33	K17	R1
DCLK (4)	93	132	152	J3	N25
CONF_DONE (4)	58	83	93	U8	AE15
INIT_DONE (5)	121	178	206	E11	A16
nCE (4)	91	130	150	K2	P26
nCEO (4)	128	185	213	C10	A12
nWS (6)	103	145	164	K5	H22
nRS (6)	102	142	161	J6	H24
nCS (6)	101	141	160	H5	J24
CS (6)	98	138	157	M2	K25
RDYnBSY (6)	120	177	205	E10	B16
CLKUSR (6)	119	176	204	F10	C16
DATA7 (6)	104	146	166	H6	G23
DATA6 (6)	105	150	169	G4	F24
DATA5 (6)	109	157	181	B2	C24
DATA4 (6)	111	160	185	C5	A25
DATA3 (6)	112	163	189	B6	B22
DATA2 (6)	115	168	195	E8	B20
DATA1 (6)	117	173	200	F9	B18
DATA0 (4), (7)	94	133	153	J2	M26
TDI (4)	90	129	149	K3	P25
TDO (4)	123	180	208	C9	B15
TCK (4)	52	76	87	U10	AE12
TMS (4)	51	75	86	U11	AF11
TRST (4)	129	186	214	B10	B12
Dedicated Inputs	56, 53, 124, 127	81, 77, 181, 184	91, 88, 209, 212	B9, D10, T9, T10	A13,A15,AF12,AE14
LOCK (8)	80	119	138	N2	P3
CLK2 (9)	92	131	151	J4	N26

Table 54. EP20K100 Device Pin-Outs (Part 2 of 2) *Note (1)*					
Pin Name	**144-Pin TQFP**	**208-Pin PQFP** *(2)*	**240-Pin PQFP** *(3)*	**324-Pin FineLine BGA** *(1)*	**356-Pin BGA EP20K100** *(1)*
CLK1	20	27	31	K16	T24
DEV_CLRn *(5)*	97	137	156	L5	L23
DEV_OE *(5)*	84	124	143	L4	R26
VCCINT	125, 108, 86, 73, 55, 36, 21, 16, 1	182, 156, 126, 105, 79, 52, 28, 23, 1	1, 27, 32, 60, 90, 122, 145, 179, 210	F7, G6, G11, H9, H12, J8, K11, K12, L7, L10, M8, M13, N5, N12	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, P4, R2, T22, U4, Y26
VCCIO	144, 116, 89, 61, 28	136, 86, 80, 53, 8, 208, 189, 172	12, 45, 67, 97, 120, 148, 177, 199, 229	E6, F5, F12, G8, G13, H7, H10, J11, K8, L9, L12, M6, M11, N7, N14, P6, P13	C26, M22, P22, AD26, AF26, AF216, AD14, AD12, AF1, AD1, P5, M5, C1, A1, C12, C14, A26
VCC_CKLK *(10)*	85	125	144	J7	P23
GNDINT	126, 87, 77, 74, 54, 34, 17, 4	183, 143, 127, 118, 78, 39, 24, 16	19, 28, 42, 89, 137, 146, 162, 211	G9, D4, D15, E5, E14, F6, F13, G7, G12, H8, H11, J9, J10, K9, K10, L8, L11, M7, M12, N6, N13, P5, P14, R4, R15	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24
GNDIO	134, 106, 72, 42, 12	199, 169, 149, 114, 95, 64, 43, 10	26, 56, 78, 108, 132, 165, 188, 218, 240	–	-
GND_CKLK *(10)*	88	128	147	K7	P24
No Connect (N.C.)	–	–	–	–	AA26, AA25, AA3, AA2, AA1, AA24, AA23, AB26, AB2, AB1, AB24, AB23, AB22, AC26, AC25, AC2, AC1, D2, D1, E4, E3, E2, J25, K26, K23
Total User I/O Pins *(11)*	101	159	189	252	252

Notes:
(1) All pins that are not listed are user I/O pins.
(2) EP20K100 devices in 208-pin QFP packages are pin-compatible with EP20K200 devices in the same package if pins 154, 148, 121, 109, 48, 36, 11, and 3 are tri-stated and connected to VCCINT, and if pins 153, 147, 110, 47, 35, 12, and 4 are tri-stated and connected to GNDINT. The Quartus software performs this function automatically when future migration is set.
(3) EP20K100 devices in 240-pin QFP packages are pin-compatible with EP20K200 devices in the same package if pins 176, 168, 140, 127, 52, 39, 14, and 5 are tri-stated and connected to VCCINT, and if pins 175, 167, 128, 51, 38, 15, and 6 are tri-stated and connected to GNDINT. The Quartus software performs this function automatically when future migration is set.
(4) This pin is a dedicated pin; it is not available as a user I/O pin.
(5) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(6) This pin can be used as a user I/O pin after configuration.
(7) This pin is tri-stated in user mode.
(8) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(9) This pin drives the ClockLock and ClockBoost circuitry.
(10) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(11) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 55 shows the pin names and numbers for EP20K200 devices in 208-pin RQFP, 240-pin RQFP, and 484-Pin FineLine BGA packages.

Table 55. EP20K200 Device Pin-Outs (Part 1 of 3) *Note (1)*

Pin Name	208-Pin RQFP *(2)*	240-Pin RQFP *(3)*	484-Pin FineLine BGA
MSEL0 *(4)*	25	29	L19
MSEL1 *(4)*	26	30	L18
NSTATUS *(4)*	82	92	W11
NCONFIG *(4)*	29	33	M19
DCLK *(4)*	132	152	L5
CONF_DONE *(4)*	83	93	W10
INIT_DONE *(5)*	178	206	G13
nCE *(4)*	130	150	M4
nCEO *(4)*	185	213	E12
nWS *(6)*	145	164	M7
nRS *(6)*	142	161	L8
nCS *(6)*	141	160	K7
CS *(6)*	138	157	P4
RDYnBSY *(6)*	177	205	G12
CLKUSR *(6)*	176	204	H12
DATA7 *(6)*	146	166	K8

Table 55. EP20K200 Device Pin-Outs (Part 2 of 3) *Note (1)*

Pin Name	208-Pin RQFP *(2)*	240-Pin RQFP *(3)*	484-Pin FineLine BGA
DATA6 *(6)*	150	169	J6
DATA5 *(6)*	157	181	D4
DATA4 *(6)*	160	185	E7
DATA3 *(6)*	163	189	D8
DATA2 *(6)*	168	195	G10
DATA1 *(6)*	173	200	H11
DATA0 *(4)*, *(7)*	133	153	L4
TDI *(4)*	129	149	M5
TDO *(4)*	180	208	E11
TCK *(4)*	76	87	W12
TMS *(4)*	75	86	W13
TRST *(4)*	186	214	D12
Dedicated Inputs	81, 77, 181, 184	91, 88, 209, 212	D11, F12, V11, V12
Dedicated Clock Pins	27, 131	31, 151	L6, M18
LOCK *(8)*	119	138	R4
CLK2 *(9)*	131	151	L6
DEV_CLRn *(5)*	137	156	N7
DEV_OE *(5)*	124	143	N6
VCCINT	1, 3, 11, 23, 28, 36, 48, 52, 79, 105, 109, 121, 126, 148, 154, 156, 182	1, 5, 14, 27, 32, 39, 52, 60, 90, 122, 127, 140, 145, 168, 176, 179, 210	AA1, AA22, B1, B22, H9, J8, J13, K11, K14, L10, M13, M14, M22, N9, N12, P10, P15, R7, R14
VCCIO	8, 53, 80, 86, 136, 172, 189, 208	12, 45, 67, 97, 120, 148, 177, 199, 229	G8, H7, H14, J10, J15, K9, K12, L1, L13, L22, M10, N11, N14, P8, P13, R9, R16, T8, T15
VCC_CKLK *(10)*	125	144	L9
GNDINT	4, 12, 16, 24, 35, 39, 47, 78, 110, 118, 127, 143, 147, 153, 183	6, 15, 19, 28, 38, 42, 51, 89, 128, 137, 146, 162, 167, 175, 211	A1, A11, A22, AA2, AA21, AB1, AB11, AB22, B2, B21, F6, F17, G7, G16, H8, H15, J9, J11, J14, K10, K13, L2, L11, L12, M1, M11, M12, M21, N10, N13, P9, P14, R8, R15, T7, T16, U6, U17
GNDIO	10, 43, 64, 95, 114, 149, 169, 199	26, 56, 78, 108, 132, 165, 188, 218, 240	–
GND_CKLK *(10)*	128	147	M9

Table 55. EP20K200 Device Pin-Outs (Part 3 of 3) *Note (1)*			
Pin Name	**208-Pin RQFP** *(2)*	**240-Pin RQFP** *(3)*	**484-Pin FineLine BGA**
No Connect (N.C.)	–	–	A9, A10, A12, A13, A14, AB9, AB10, AB12, AB13, AB14
Total User I/O Pins *(11)*	144	174	382

Notes:
(1) All pins that are not listed are user I/O pins.
(2) EP20K100 devices in 208-pin QFP packages are pin-compatible with EP20K200 devices in the same package if pins 154, 148, 121, 109, 48, 36, 11, and 3 are tri-stated and connected to VCCINT, and if pins 153, 147, 110, 47, 35, 12, and 4 are tri-stated and connected to GNDINT. The Quartus software performs this function automatically when future migration is set.
(3) EP20K100 devices in 240-pin QFP packages are pin-compatible with EP20K200 devices in the same package if pins 176,168,140, 127, 52, 39, and 5 are tri-stated and connected to VCCINT, and if pins 175, 167, 128, 51, 38, 15, and 6 are tri-stated and connected to GNINT. The Quartus software performs this function automatically when future migration is set.
(4) This pin is a dedicated pin; it is not available as a user I/O pin.
(5) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(6) This pin can be used as a use I/O pin after configuration.
(7) This pin is tri-stated in user mode.
(8) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, Lock is driven high. Lock remains high if a periodic clock stops clocking. The Lock function is optional; if the Lock output is not used, this pin is a user I/O pin.
(9) This pin drives the ClockLock and ClockBoost circuitry.
(10) This pin is the power or ground for the CLockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(11) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 56 shows the pin names and numbers for EP20K400 devices in 652-pin BGA, 655-pin PGA, and 672-pin FineLine BGA packages.

Table 56. EP20K400 Device Pin-Outs (Part 1 of 3) *Note (1)*

Pin Name	652-Pin BGA	655-Pin PGA	672-Pin FineLine BGA
MSEL0 *(2)*	U35	A23	N21
MSEL1 *(2)*	W35	C23	N20
NSTATUS *(2)*	AN17	AE41	AA13
NCONFIG *(2)*	W32	C25	P21
DCLK *(2)*	U3	BA23	N7
CONF_DONE *(2)*	AM17	AC47	AA12
INIT_DONE *(3)*	C16	AE7	J15
nCE *(2)*	U1	BE25	P6
nCEO *(2)*	C19	AC9	G14
nWS *(4)*	M1	BF14	P9
nRS *(4)*	N1	AY20	N10
nCS *(4)*	P2	BB20	M9
CS *(4)*	R2	BD20	T6
RDYnBSY *(4)*	A14	AH4	J14
CLKUSR *(4)*	C15	AH6	K14
DATA7 *(4)*	M6	BG13	M10
DATA6 *(4)*	L6	BB16	L8
DATA5 *(4)*	E7	BC3	F6
DATA4 *(4)*	B5	AR7	G9
DATA3 *(4)*	B7	AV4	F10
DATA2 *(4)*	A8	AP6	J12
DATA1 *(4)*	C13	AH8	K13
DATA0 *(2)*, *(5)*	U4	BE23	N6
TDI *(2)*	W1	BG23	P7
TDO *(2)*	C17	AE1	G13
TCK *(2)*	AN19	AC45	AA14
TMS *(2)*	AM19	AD40	AA15
TRST *(2)*	D19	AD2	F14
Dedicated Inputs	B17, B19, AP17, AP19	AB4, AC5, AC43, AE43	F13, H14, Y13, Y14
Dedicated Clock Pins	U2, W34	H24, AY24	N8, P20
LOCK *(6)*	AB6	BG29	U6
CLK2 *(7)*	U2	AY24	N8
DEV_CLRn *(3)*	T6	AY22	R9
DEV_OE *(3)*	Y5	BF26	R8

Table 56. EP20K400 Device Pin-Outs (Part 2 of 3) *Note (1)*

Pin Name	652-Pin BGA	655-Pin PGA	672-Pin FineLine BGA
VCCINT	A17, A19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N4, N35 R5, R34, U5, U34, W3, W31, W33, AA4, AA31, AC3, AC32, AE2, AE33, AG1, AH4, AH31, AH35, AK33, AL2, AL12, AL24, AM12, AM24, AR17, AR19	A3, A45, B24, C1, C11, C19, C29, C37, C47, D24, G47, L3, L45, N1, N47, W3, W45, AA1, AA47, AD4, AD44, AG1, AG47, AJ3, AJ45, AR1, AR47, AU3, AU45, AY8, BA1, BA47, BD24, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P16, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO	AL3, AL4, AL17, AL19, AL31, AL32, AM5, AN4, AN32, AN33, C4, C32, D5, D31, E3, E4, E17, E19, F30, F31, U6, U30, W6, W30,	E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39	A6, A13, A21, J10, K9, K16, L12, L17, M11, M14, N3, N15, N24, P12, R13, R16, T10, T15, U11, U18, V10, V17, AF6, AF13, AF21
VCC_CKLK *(8)*	W4	BD28	N11
GNDINT	A1, A18, A35, B1, B2, B18, B34, B35, C2, C3, C18, C33, C34, C35, D2, D3, D4, D17, D18, D32, D33, D34, E5, E6, E18, E30, E31, E32, E33, F18, V1, V2, V3, V4, V5, V6, V30, V31, V32, V33, V34, V35, AK18, AL5, AL6, AL18, AL30, AM18, AM2, AM3, AM4, AM31, AM32, AM33, AM34, AN1, AN2, AN3, AN18, AN34, AN35, AP1, AP2, AP18, AP34, AP35, AR1, AR18, AR35,	A47, B2, C13, C21, C27, C35, C45, D4, F24, J1, J47, N3, N45, R1, R47, W1, W47, AA3, AA45, AD6, AD8, AD42, AG3, AG45, AJ1, AJ47, AN1, AN47, AR3, AR45, AW1, AW47, BB24, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N25, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25
GNDIO	–	E7, E13, E19, E29, E35, E41, G5, G43, H40, N5, N43, W5, W43, AJ5, AJ43, AR5, AR43, AY40, BA5, BA43, BC7, BC13, BC19, BC29, BC35, BC41, BF46	–
GND_CKLK *(8)*	W2	BD26	P11

Table 56. EP20K400 Device Pin-Outs (Part 3 of 3) *Note (1)*			
Pin Name	**652-Pin BGA**	**655-Pin PGA**	**672-Pin FineLine BGA**
No Connect (N.C.)	–	–	A15, A16, B13, B14, B15, B16, C11, C12, C14, C15, C16, AD11, AD12, AD14, AD15, AD16, AE12, AE13, AE14, AE15, AF12, AF15,
Total User I/O Pins *(9)*	502	502	502

Notes:
(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(7) This pin drives the ClockLock and ClockBoost circuitry.
(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(9) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.

Table 57 shows I/O pin information for EP20K100E devices in 144-pin TQFP, 208-pin RQFP, and 240-pin RQFP packages.

Table 57. EP20K100E I/O Pin-Outs (Part 1 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
8	1	I/O	–	–	180
8	2	I/O	–	155	178
8	3	I/O	–	–	–
–	4	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	5	I/O	–	–	–
–	6	VCCINT	VCCINT	VCCINT	VCCINT
8	7	I/O	–	154	176
8	8	I/O	–	–	175
8	9	I/O	–	153	174
8	10	I/O	–	–	173
8	11	I/O	–	152	172
–	12	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	13	I/O	–	–	171
8	14	I/O	–	–	–
8	15	I/O	–	151	170
8	16	I/O	–	–	–
8	17	I/O, DATA6 *(2)*	105	150	169
–	18	GNDINT	GND	GND	GND
8	19	I/O	–	–	–
8	20	I/O	–	148	168
8	21	I/O	–	147	167
8	22	I/O	–	–	–
8	23	I/O, DATA7 *(2)*	104	146	166
–	24	GNDIO	GND	GND	GND
8	25	I/O, nWS *(2)*	103	145	164
8	26	I/O	–	–	–
8	27	I/O	–	144	163
8	28	I/O, nRS *(2)*	102	142	161
8	29	I/O, nCS *(2)*	101	141	160
–	30	VCCINT	VCCINT	VCCINT	VCCINT
–	31	VCC_CKLK4 *(3)*	100	140	159
–	32	GND_CKLK4 *(3)*	99	139	158

Table 57. EP20K100E I/O Pin-Outs (Part 2 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
–	33	GND_CKLK4 *(3)*	99	139	158
8	34	I/O	–	–	–
8	35	I/O, CS *(2)*	98	138	157
8	36	I/O, DEV_CLRn *(4)*	97	137	156
–	37	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	38	I/O, CLKLK_FB2n *(5)*	–	–	–
8	39	CLKLK_FB2p	96	135	155
8	40	I/O, CLK4n *(5)*	–	–	–
8	41	CLK4p	95	134	154
8	42	I/O, CLK2n *(5)*	–	–	–
–	43	DATA0 *(6)*	94	133	153
–	44	DCLK *(6)*	93	132	152
8	45	CLK2p	92	131	151
–	46	nCE *(6)*	91	130	150
–	47	TDI *(6)*	90	129	149
–	48	VCCIO	VCCIO7	VCCIO7	VCCIO7
–	49	GND_CKLK2 *(3)*	88	128	147
–	50	GND_CKLK2 *(3)*	88	128	147
–	51	GNDINT	GND	GND	GND
–	52	VCC_CKLK2 *(3)*	85	125	144
7	53	I/O, DEV_OE *(4)*	84	124	143
–	54	VCC_CKOUT2 *(7)*	83	123	142
–	55	GND_CKOUT2 *(7)*	82	122	141
7	56	I/O	–	–	–
7	57	I/O	–	121	140
–	58	GNDIO	GND	GND	GND
–	59	CLKLK_OUT2p	81	120	139
7	60	I/O, CLKLK_OUT2n *(5)*	–	–	–
7	61	I/O, LOCK2 *(8)*	80	119	138
7	62	I/O	–	–	–
7	63	I/O	79	117	136
–	64	VCCINT	VCCINT	VCCINT	VCCINT
7	65	I/O, LOCK4 *(8)*	78	116	135
7	66	I/O	–	–	–

Table 57. EP20K100E I/O Pin-Outs (Part 3 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
7	67	I/O	–	–	134
7	68	I/O	–	–	–
7	69	I/O	–	–	133
–	70	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	71	I/O	–	–	–
7	72	I/O	–	–	131
7	73	I/O	–	–	130
7	74	I/O	–	113	129
7	75	I/O	–	112	128
–	76	GNDINT	GND	GND	GND
7	77	I/O	76	111	127
7	78	I/O	–	–	–
7	79	I/O	75	110	126
7	80	I/O	–	–	–
7	81	I/O	–	109	125
–	82	GNDIO	GND	GND	GND
–	83	VCCINT	VCCINT	VCCINT	VCCINT
7	84	I/O	–	108	124
7	85	I/O	–	–	–
7	86	I/O	–	107	123
7	87	I/O	–	106	121
–	88	VCCIO	VCCIO7	VCCIO7	VCCIO7
–	89	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	90	I/O	71	104	119
6	91	I/O	–	–	118
6	92	I/O	–	103	117
6	93	I/O	70	102	116
6	94	I/O	–	–	–
6	95	I/O	69	101	115
6	96	I/O	–	–	–
6	97	I/O	68	100	114
6	98	I/O	–	99	113
6	99	I/O	–	–	112
–	100	GNDIO	GND	GND	GND
6	101	I/O	67	98	111

Table 57. EP20K100E I/O Pin-Outs (Part 4 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
6	102	I/O	–	97	110
6	103	I/O	66	96	109
6	104	I/O	–	–	–
6	105	I/O	65	94	107
6	106	I/O	–	–	106
6	107	I/O	–	93	105
6	108	I/O	–	–	104
6	109	I/O	64	92	103
6	110	I/O	–	–	–
–	111	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	112	I/O	63	91	102
6	113	I/O	–	90	101
6	114	I/O	–	–	–
6	115	I/O	62	89	100
6	116	I/O	–	88	99
6	117	I/O	–	87	98
–	118	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	119	I/O	60	85	96
6	120	I/O	59	84	95
6	121	I/O	–	–	–
6	122	I/O	–	–	94
–	123	CONF_DONE *(6)*	58	83	93
–	124	nSTATUS *(6)*	57	82	92
5	125	FAST4	56	81	91
–	126	VCCIO	VCCIO5	VCCIO5	VCCIO5
–	127	GNDINT	GND	GND	GND
–	128	GNDINT	–	–	–
–	129	VCCINT	VCCINT	VCCINT	VCCINT
–	130	VCCINT	VCCINT	VCCINT	VCCINT
–	131	GNDINT	–	–	–
–	132	GNDINT	GND	GND	GND
–	133	GNDIO	GND	GND	GND
5	134	FAST3	53	77	88
–	135	TCK *(6)*	52	76	87
–	136	TMS *(6)*	51	75	86

Table 57. EP20K100E I/O Pin-Outs (Part 5 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
5	137	I/O	50	74	85
5	138	I/O	–	73	84
5	139	I/O	–	–	83
5	140	I/O	49	72	82
5	141	I/O	–	–	–
5	142	I/O	48	71	81
5	143	I/O	–	–	80
5	144	I/O	47	70	79
5	145	I/O	–	69	77
5	146	I/O	46	68	76
–	147	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	148	I/O	–	67	75
5	149	I/O	–	–	–
5	150	I/O	–	66	74
5	151	I/O	44	65	73
5	152	I/O	–	–	–
5	153	I/O	–	63	72
5	154	I/O	43	62	71
5	155	I/O	–	–	70
5	156	I/O	–	61	69
5	157	I/O	41	60	68
–	158	GNDIO	GND	GND	GND
–	159	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	160	I/O	40	59	66
5	161	I/O	–	–	–
5	162	I/O	–	58	65
5	163	I/O	–	–	–
5	164	I/O	39	57	64
5	165	I/O	–	–	–
5	166	I/O	38	56	63
5	167	I/O	–	55	62
5	168	I/O	–	–	–
5	169	I/O	37	54	61
–	170	VCCIO	VCCIO5	VCCIO5	VCCIO5
–	171	VCCIO	VCCIO4	VCCIO4	VCCIO4

Table 57. EP20K100E I/O Pin-Outs (Part 6 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
4	172	I/O	–	51	59
4	173	I/O	35	50	58
4	174	I/O	–	–	–
4	175	I/O	–	49	57
–	176	GNDINT	GND	GND	GND
–	177	GNDIO	GND	GND	GND
4	178	I/O	–	48	55
4	179	I/O	–	–	54
4	180	I/O	33	47	53
4	181	I/O	–	–	52
4	182	I/O	32	46	51
–	183	VCCINT	VCCINT	VCCINT	VCCINT
4	184	I/O	31	45	50
4	185	I/O	–	–	49
4	186	I/O	30	44	48
4	187	I/O	–	–	47
4	188	I/O	29	–	46
–	189	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	190	I/O	27	41	44
4	191	I/O	–	–	–
4	192	I/O	26	40	43
4	193	I/O	–	38	41
4	194	I/O	–	37	40
–	195	GNDINT	GND	GND	GND
4	196	I/O	–	36	39
4	197	I/O	–	35	38
4	198	I/O	25	34	37
4	199	I/O	–	–	–
4	200	I/OI/O	24	33	36
–	201	GNDIO	GND	GND	GND
4	202	I/O	–	–	–
4	203	I/O	–	32	35
4	204	I/O, CLK3n *(5)*	–	–	–
4	205	CLK3p	23	31	34
4	206	I/O, CLK1n*(5)*	–	30	–

Table 57. EP20K100E I/O Pin-Outs (Part 7 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
–	207	VCCINT	VCCINT	VCCINT	VCCINT
–	208	nCONFIG *(6)*	22	29	33
–	209	CLKLK_ENA *(6)*, *(9)*	21	28	32
4	210	CLK1p	20	27	31
–	211	MSEL1 *(6)*	19	26	30
–	212	MSEL0 *(6)*	18	25	29
3	213	I/O	–	–	–
3	214	I/O	–	–	–
3	215	I/O	15	22	25
3	216	I/O	–	–	–
3	217	I/O	–	–	–
–	218	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	219	I/O	14	21	24
3	220	I/O	–	–	–
3	221	I/O	13	20	23
3	222	I/O	–	–	–
3	223	I/O	–	19	22
–	224	GNDINT	GND	GND	GND
3	225	I/O	–	18	21
3	226	I/O	–	–	–
3	227	I/O	11	17	20
3	228	I/O	–	15	18
3	229	I/O	10	14	17
–	230	GNDIO	GND	GND	GND
3	231	I/O	–	–	16
3	232	I/O	–	–	15
3	233	I/O	9	13	14
3	234	I/O	–	–	–
3	235	I/O	8	12	13
–	236	VCCINT	VCCINT	VCCINT	VCCINT
–	237	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	238	I/O	–	–	11
3	239	I/O	–	–	–
3	240	I/O	7	11	10
3	241	I/O	–	–	–

Table 57. EP20K100E I/O Pin-Outs (Part 8 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
3	242	I/O	6	9	9
–	243	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	244	I/O	–	–	8
3	245	I/O	–	7	7
3	246	I/O	–	6	6
3	247	I/O	–	–	–
3	248	I/O	–	5	5
–	249	GNDINT	GND	GND	GND
3	250	I/O	3	4	4
3	251	I/O	–	–	–
3	252	I/O	2	3	3
3	253	I/O	–	2	2
–	254	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	255	GNDIO	GND	GND	GND
2	256	I/O	143	207	239
2	257	I/O	–	–	238
2	258	I/O	142	206	237
2	259	I/O	–	–	–
2	260	I/O	–	205	236
2	261	I/O	–	–	–
2	262	I/O	141	204	235
2	263	I/O	–	–	–
2	264	I/O	–	203	234
2	265	I/O	140	202	233
–	266	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	267	I/O	139	201	232
2	268	I/O	–	200	231
2	269	I/O	138	198	230
2	270	I/O	–	–	–
–	271	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	272	I/O	137	197	228
2	273	I/O	–	–	–
2	274	I/O	–	196	227
2	275	I/O	136	195	226
2	276	I/O	–	–	225

Table 57. EP20K100E I/O Pin-Outs (Part 9 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
2	277	I/O	135	194	224
–	278	GNDIO	GND	GND	GND
2	279	I/O	–	193	223
2	280	I/O	133	192	222
2	281	I/O	–	–	221
2	282	I/O	132	191	220
2	283	I/O	–	–	–
2	284	I/O	–	190	219
–	285	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	286	I/O	–	–	–
2	287	I/O	131	188	217
2	288	I/O	–	–	216
2	289	I/O	130	187	215
–	290	TRST *(6)*	129	186	214
–	291	NCEO	128	185	213
1	292	FAST1	127	184	212
–	293	GNDINT	GND	GND	GND
–	294	GNDINT	–	–	–
–	295	VCCINT	VCCINT	VCCINT	VCCINT
–	296	VCCINT	VCCINT	VCCINT	VCCINT
–	297	GNDINT	GND	GND	GND
–	298	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	299	FAST2	124	181	209
–	300	TDO *(6)*	123	180	208
–	301	GNDINT	–	–	–
1	302	I/O	122	179	207
1	303	I/O, INITDONE *(2)*	121	178	206
1	304	I/O, RDYnBSY *(2)*	120	177	205
1	305	I/O	–	–	–
1	306	I/O, CLKUSR *(2)*	119	176	204
1	307	I/O	–	–	203
1	308	I/O	118	175	202
1	309	I/O	–	174	201
1	310	I/O, DATA1 *(2)*	117	173	200
1	311	I/O	–	–	–

Table 57. EP20K100E I/O Pin-Outs (Part 10 of 10) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP	208-Pin RQFP	240-Pin RQFP
–	312	GNDIO	GND	GND	GND
–	313	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	314	I/O	–	171	198
1	315	I/O	–	–	197
1	316	I/O	–	170	196
1	317	I/O, DATA2 *(2)*	115	168	195
1	318	I/O	–	167	–
1	319	I/O	114	166	194
1	320	I/O	–	165	193
1	321	I/O	113	164	192
1	322	I/O	–	–	–
1	323	I/O	–	–	191
–	324	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	325	I/O	–	–	190
1	326	I/O, DATA3 *(2)*	112	163	189
1	327	I/O	–	162	187
1	328	I/O	–	161	186
1	329	I/O	–	–	–
1	330	I/O, DATA4 *(2)*	111	160	185
1	331	I/O	–	159	184
1	332	I/O	110	158	183
1	333	I/O	–	–	182
1	334	I/O, DATA5*(2)*	109	157	181
–	335	GNDIO	GND	GND	GND

Table 58 shows configuration and power pin information for EP20K100E devices in 144-pin TQFP, 208-pin RQFP, and 240-pin RQFP packages.

Table 58. EP20K100E Configuration & Power Pins (Part 1 of 2)

Pin Name	144-Pin TQFP (1)	208-Pin RQFP(1)	240-Pin RQFP (1)
MSEL0 (6)	18	25	29
MSEL1 (6)	19	26	30
NSTATUS (6)	57	82	92
NCONFIG (6)	22	29	33
DCLK (6)	93	132	152
CONF_DONE (6)	58	83	93
INIT_DONE (4)	121	178	206
nCE (6)	91	130	150
nCEO (6)	128	185	213
nWS (2)	103	145	164
nRS (2)	102	142	161
nCS (2)	101	141	160
CS (2)	98	138	157
RDYnBSY (2)	120	177	205
CLKUSR (2)	119	176	204
DATA7 (2)	104	146	166
DATA6 (2)	105	150	169
DATA5 (2)	109	157	181
DATA4 (2)	111	160	185
DATA3 (2)	112	163	189
DATA2 (2)	115	168	195
DATA1 (2)	117	173	200
DATA0 (6), (11)	94	133	153
TDI (6)	90	129	149
TDO (6)	123	180	208
TCK (6)	52	76	87
TMS (6)	51	75	86
TRST (6)	129	186	214
Dedicated Fast I/Os	53, 56, 124, 127	77, 81, 181, 184	88, 91, 209, 212
CLK1p	20	27	31
CLK2p	92	131	151
CLK3p	23	31	34
CLK4p	95	134	154
LOCK2 (8)	80	119	138

Table 58. EP20K100E Configuration & Power Pins (Part 2 of 2)

Pin Name	144-Pin TQFP *(1)*	208-Pin RQFP*(1)*	240-Pin RQFP *(1)*
LOCK4 *(8)*	78	116	135
CLKLK_ENA *(6)*, *(9)*	21	28	32
CLKLK_OUT2p	81	120	139
CLKLK_FB2p	96	135	155
DEV_CLRn *(4)*	97	137	156
DEV_OE *(4)*	84	124	143
VCCINT	1, 16, 36, 55, 73, 86, 108, 125	1, 23, 52, 79, 105, 126, 156, 182	1, 27, 60, 90, 122, 145, 179, 210
VCCIO1	116	172	199
VCCIO2	144	208	229
VCCIO3	5	8,189	12
VCCIO4	45	80	67
VCCIO5	28	42,53	45
VCCIO6	89	115	148
VCCIO7	61	86	97,120
VCCIO8	107	136	177
VCC_CKLK2 *(12)*	85	125	144
VCC_CKLK4 *(12)*	100	140	159
VCC_CKOUT2 *(7)*	83	123	142
GND	4, 12, 17, 34, 42, 54, 72, 74, 77, 87, 106, 126, 134	10, 16, 24, 39, 43, 64, 78, 95, 114, 118, 127, 143, 149, 169, 183, 199	19, 26, 28, 42, 56, 78, 89, 108, 132, 137, 146, 162, 165, 188, 211, 218, 240
GND_CKLK2 *(12)*	88	128	147
GND_CKLK4 *(3)*	99	139	158
GND_CKOUT2 *(7)*	82	122	141
No Connect (N.C.)	–	–	–
Total User I/O Pins *(10)*	92	151	183

Notes to tables:

(1) For the 144-pin, 208-pin, and 240-pin QFP packages, Four unique VCCIO levels are supported. The VCCIOs for I/O bank 1 and 8 must be at the same level; the VCCIOs for I/O banks 7 and 6 must be at the same level; the VCCIOs for I/O banks 3 and 2 must be at the same level. However, unique VREF settings are supported for each of the eight I/O banks.
(2) This pin can be used as a user I/O pin after configuration.
(3) The CLKLK_OUT and CLKLK_FBIN pins are powered by the VCC_CKOUT and GND_CKOUT pins.
(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for LVDS standard. If not used for the LVDS pair, these pins are regular I/Os. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.
(6) This pin is a dedicated pin; it is not available as a user I/O pin.
(7) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(8) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(9) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will begin lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.
(10) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.
(11) This pin is tri-stated in user mode.
(12) This pin is the power or ground for the external output and feedback input of a PLL. These pins should be set to the V_{CCIO} level/standard desired for the external clock output and feedback input (if used). To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the V_{CCIO} and GND_{IO} pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

Table 59 shows I/O pin information for EP20K200E devices in 208-pin RQFP, 240-pin RQFP, 484-pin FineLine BGA, 672-pin FineLine BGA, and 652-pin BGA packages.

Table 59. EP20K200E I/O Pins (Part 1 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
8	1	I/O	–	–	B11	F6	E5
8	2	I/O	155	180	B10	F5	E3
8	3	I/O	–	–	B9	F4	F5
8	4	I/O	–	–	A8	C1	F4
–	5	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	6	I/O	–	–	B8	D1	E4
8	7	I/O	–	–	A7	E2	F3
8	8	I/O	152	178	B7	G6	D5
8	9	I/O	–	–	B6	G5	G5

Table 59. EP20K200E I/O Pins (Part 2 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
8	10	I/O	–	–	A6	G4	G3
–	11	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	12	I/O	–	174	A5	G3	G8
8	13	I/O	–	–	B5	F2	G4
8	14	I/O	151	173	B4	E1	C4
8	15	I/O	–	–	A3	G2	G6
8	16	I/O	–	–	A4	H6	H5
–	17	GNDINT	GND	GND	GND	GND	GND
8	18	I/O	–	172	C3	H4	G7
8	19	I/O	–	–	C1	H3	H7
8	20	I/O	–	171	D3	F1	H4
8	21	I/O	–	–	D2	H2	H6
8	22	I/O	–	–	C2	G1	K7
–	23	GNDIO	GND	GND	GND	GND	GND
8	24	I/O	–	170	D1	J6	J5
8	25	I/O	–	–	B3	J5	H9
8	26	I/O, DATA6 *(2)*	150	169	J6	L6	L8
8	27	I/O	–	–	E3	J4	H3
8	28	I/O	–	–	E1	J3	K3
–	29	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	30	I/O	–	–	E6	J2	J4
8	31	I/O	–	–	E2	J1	K5
8	32	I/O, DATA7 *(2)*	146	166	K8	M6	M10
8	33	I/O	–	–	A2	K6	L6
8	34	I/O	–	–	E4	K5	J7
–	35	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	36	I/O	–	–	F3	K4	J3
8	37	I/O	–	–	E5	K3	K8
8	38	I/O, nWS *(2)*	145	164	M7	M1	P9
8	39	I/O	–	–	F5	K2	K6
8	40	I/O	–	–	F2	K1	K4
–	41	GNDINT	GND	GND	GND	GND	GND
8	42	I/O	–	–	F4	L5	N5
8	43	I/O	–	–	H5	L4	M8
8	44	I/O	144	163	G3	L2	J8

Table 59. EP20K200E I/O Pins (Part 3 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
8	45	I/O	–	–	F7	L1	M6
8	46	I/O	–	–	G6	M5	L7
–	47	GNDIO	GND	GND	GND	GND	GND
8	48	I/O	–	–	F1	M4	L9
8	49	I/O	–	–	H1	M3	M7
8	50	I/O, nRS *(2)*	142	161	L8	N1	N10
8	51	I/O	–	–	G2	M2	L5
8	52	I/O	–	–	H3	N6	P8
–	53	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	54	I/O	–	–	G4	N5	L4
8	55	I/O	–	–	J4	N3	L3
8	56	I/O, nCS *(2)*	141	160	K7	P2	M9
8	57	I/O	–	–	G5	N2	R4
8	58	I/O	–	–	G1	P6	M5
–	59	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	60	I/O	–	–	H6	P5	M3
8	61	I/O	–	–	H4	P4	P4
8	62	I/O	–	–	H2	P3	J6
8	63	I/O	–	–	L3	P1	R3
8	64	I/O	–	–	K6	R6	P5
–	65	GNDINT	GND	GND	GND	GND	GND
–	66	VCC_CKLK4 *(3)*	140	159	M8	R4	P10
–	67	GND_CKLK4 *(3)*	139	158	N8	R3	R10
–	68	GND_CKLK4 *(3)*	139	158	N8	R3	R10
8	69	I/O, CS *(2)*	138	157	P4	R2	T6
8	70	I/O	–	–	K4	R1	M4
8	71	I/O, DEV_CLRn *(4)*	137	156	N7	T6	R9
–	72	VCCIO	VCCIO8	VCCIO8	–	VCCIO8	–
–	73	GNDIO	GND	GND	GND	GND	GND
8	74	I/O, CLKLK_FB2n *(5)*	–	–	P6	T5	T8
–	75	CLKLK_FB2p *(6)*	135	155	R6	T4	U8

Table 59. EP20K200E I/O Pins (Part 4 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
8	76	I/O, CLK4n *(5)*	–	–	N5	T3	R7
–	77	CLK4p	134	154	N4	T2	R6
8	78	I/O, CLK2n *(5)*	–	–	L7	T1	N9
–	79	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	80	DATA0 *(7)*, *(8)*	133	153	L4	U4	N6
–	81	DCLK *(7)*	132	152	L5	U3	N7
–	82	CLK2p	131	151	L6	U2	N8
–	83	NCE *(7)*	130	150	M4	U1	P6
–	84	TDI *(7)*	129	149	M5	W1	P7
–	85	VCCIO	VCCIO7	VCCIO7	–	VCCIO7	–
–	86	GND_CKLK2 *(3)*	128	147	M9	W2	P11
–	87	GND_CKLK2 *(3)*	128	147	M9	W2	P11
–	88	GNDINT	GND	GND	GND	GND	GND
–	89	VCC_CKLK2 *(3)*	125	144	L9	W4	N11
7	90	I/O, DEV_OE *(4)*	124	143	N6	Y5	R8
–	91	VCC_CKOUT2 *(9)*	123	142	T5	Y1	V7
–	92	GND_CKOUT1	122	141	T4	Y2	V6
–	93	CLKLK_OUT2p	120	139	P5	Y3	T7
7	94	I/O, CLKLK_OUT2n *(5)*	–	–	R5	Y4	U7
–	95	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	96	I/O	–	–	J5	W5	D1
7	97	I/O	–	–	J7	Y6	D2
7	98	I/O, LOCK2 *(10)*	119	138	R4	AB6	U6
7	99	I/O	–	–	K5	AA2	E1
7	100	I/O	–	–	J3	AA3	E2
–	101	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	102	I/O	–	–	M6	AA5	F1
7	103	I/O	–	–	J2	AA6	F2
7	104	I/O	–	–	J1	AB1	R5
7	105	I/O	–	–	N2	AB2	G1
7	106	I/O	–	–	K3	AB3	G2
–	107	GNDIO	GND	GND	GND	GND	GND

Table 59. EP20K200E I/O Pins (Part 5 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
7	108	I/O	117	136	K1	AB4	H1
7	109	I/O	–	–	M2	AB5	H2
7	110	I/O, LOCK4 *(10)*	116	135	U5	AC6	W7
7	111	I/O	–	–	N1	AC1	J1
7	112	I/O	–	–	M3	AC2	J2
–	113	GNDINT	GND	GND	GND	GND	GND
7	114	I/O	–	–	K2	AC4	K1
7	115	I/O	–	–	N3	AC5	K2
7	116	I/O	–	134	P3	AA1	T5
7	117	I/O	–	–	P1	AD1	L1
7	118	I/O	–	–	R3	AD2	L2
–	119	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	120	I/O	–	–	P2	AD3	M1
7	121	I/O	–	–	R2	AD4	M2
7	122	I/O	–	–	R1	AD5	T3
7	123	I/O	–	133	T1	AD6	R1
7	124	I/O	–	–	U3	AE1	R2
–	125	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	126	I/O	–	–	U4	AE3	T1
7	127	I/O	–	–	T3	AE4	T2
7	128	I/O	–	131	T2	AE5	U5
7	129	I/O	–	–	U2	AE6	U1
7	130	I/O	–	130	U1	AF1	U2
–	131	GNDIO	GND	GND	GND	GND	GND
7	132	I/O	–	–	V3	AF2	V1
7	133	I/O	–	–	Y3	AF3	V2
7	134	I/O	113	129	W3	AF4	T4
7	135	I/O	–	–	V4	AF5	W1
7	136	I/O	–	–	W4	AF6	W2
–	137	GNDINT	GND	GND	GND	GND	GND
7	138	I/O	–	–	W5	AH1	Y1
7	139	I/O	–	–	Y4	AG2	Y2
7	140	I/O	112	126	Y2	AG3	U4
7	141	I/O	–	–	W2	AG4	AA1
7	142	I/O	–	–	AA3	AG5	AA2

Table 59. EP20K200E I/O Pins (Part 6 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
–	143	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	144	I/O	–	–	V2	AG6	AB1
7	145	I/O	–	–	Y1	AJ1	AB2
7	146	I/O	111	125	V1	AH2	W4
7	147	I/O	–	–	AB2	AK1	AC1
7	148	I/O	–	–	W1	AH3	AC2
–	149	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	150	I/O	–	–	AB3	AH5	U3
7	151	I/O	–	–	AB4	AH6	V3
7	152	I/O	108	124	AA4	AJ2	W5
7	153	I/O	–	–	AA5	AL1	W6
7	154	I/O	–	–	AB5	AK2	V5
–	155	GNDIO	GND	GND	GND	GND	GND
7	156	I/O	–	–	AA6	AJ3	V4
7	157	I/O	–	–	AB6	AJ4	W3
7	158	I/O	107	123	AA7	AJ5	Y5
7	159	I/O	–	–	AB7	AJ6	AB5
7	160	I/O	–	–	AA8	AM1	AA5
–	161	GNDINT	GND	GND	GND	GND	GND
7	162	I/O	–	–	AA11	AK3	Y6
7	163	I/O	–	–	AA10	AK4	AA6
7	164	I/O	106	121	AB8	AK5	AA7
7	165	I/O	–	–	AA9	AK6	AB6
–	166	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	–
–	167	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	168	I/O	104	119	Y5	AR8	AB7
6	169	I/O	–	118	V5	AN11	Y7
6	170	I/O	103	117	Y6	AP10	AB8
6	171	I/O	102	116	T6	AR9	V8
6	172	I/O	–	–	P7	AL13	T9
6	173	I/O	101	115	W7	AM13	AA9
6	174	I/O	–	–	W6	AN12	AA8
6	175	I/O	100	114	V6	AP11	Y8
6	176	I/O	99	113	V7	AL14	Y9
6	177	I/O	–	112	U7	AR10	W9

Table 59. EP20K200E I/O Pins (Part 7 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
–	178	GNDIO	GND	GND	GND	GND	GND
6	179	I/O	98	111	Y7	AN13	AB9
6	180	I/O	97	110	U8	AP12	W10
6	181	I/O	96	109	V8	AM14	Y10
6	182	I/O	–	–	W8	AR11	AA10
6	183	I/O	94	107	Y9	AL15	AB11
6	184	I/O	–	106	T9	AN14	V11
6	185	I/O	93	105	Y8	AP13	AB10
6	186	I/O	–	104	W9	AR12	AA11
6	187	I/O	92	103	V9	AR13	Y11
6	188	I/O	–	–	U9	AM15	W11
–	189	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	190	I/O	91	102	T10	AN15	V12
6	191	I/O	90	101	U10	AL16	W12
6	192	I/O	–	–	V10	AP14	Y12
6	193	I/O	89	100	P11	AR14	T13
6	194	I/O	88	99	U12	AP15	W14
6	195	I/O	87	98	Y10	AR15	AB12
–	196	VCCIO	VCCIO6	VCCIO6	–	VCCIO6	VCCIO6
6	197	I/O	85	96	R11	AM16	U13
6	198	I/O	84	95	R10	AN16	U12
6	199	I/O	–	–	U11	AP16	W13
6	200	I/O	–	94	T11	AR16	V13
–	201	CONF_DONE *(7)*	83	93	W10	AM17	AA12
–	202	NSTATUS *(7)*	82	92	W11	AN17	AA13
5	203	FAST4	81	91	V11	AP17	Y13
–	204	VCCIO	VCCIO5	VCCIO5	–	VCCIO5	VCCIO5
–	205	GNDINT	GND	GND	GND	GND	GND
–	206	GNDINT	–	–	–	–	–
–	207	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	208	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	209	GNDINT	–	–	–	–	–
–	210	GNDINT	GND	GND	GND	GND	GND
–	211	GNDIO	GND	GND	GND	GND	GND
5	212	FAST3	77	88	V12	AP19	Y14

Table 59. EP20K200E I/O Pins (Part 8 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
–	213	TCK *(7)*	76	87	W12	AN19	AA14
–	214	TMS *(7)*	75	86	W13	AM19	AA15
5	215	I/O	74	85	Y11	AR20	AB13
5	216	I/O	73	84	T12	AP20	V14
5	217	I/O	–	83	Y12	AN20	AB14
5	218	I/O	72	82	V13	AM20	Y15
5	219	I/O	–	–	R12	AR21	U14
5	220	I/O	71	81	T13	AP21	V15
5	221	I/O	–	80	Y13	AR22	AB15
5	222	I/O	70	79	U13	AP22	W15
5	223	I/O	69	77	Y14	AL20	AB16
5	224	I/O	68	76	P12	AN21	T14
–	225	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
5	226	I/O	67	75	W14	AM21	AA16
5	227	I/O	66	74	V14	AR23	Y16
5	228	I/O	–	–	U14	AR24	W16
5	229	I/O	65	73	R13	AP23	U15
5	230	I/O	–	–	Y15	AN22	AB17
5	231	I/O	63	72	T14	AL21	V16
5	232	I/O	62	71	W15	AR25	AA17
5	233	I/O	–	70	Y16	AM22	AB18
5	234	I/O	61	69	V15	AP24	Y17
5	235	I/O	60	68	W16	AN23	AA18
–	236	GNDIO	GND	GND	GND	GND	GND
–	237	VCCIO	VCCIO5	VCCIO5	–	VCCIO5	VCCIO5
5	238	I/O	59	66	U15	AR26	W17
5	239	I/O	–	–	V16	AL22	Y18
5	240	I/O	58	65	U16	AP25	W18
5	241	I/O	–	–	W17	AN24	AA19
5	242	I/O	57	64	V17	AM23	Y19
5	243	I/O	–	–	U18	AL23	W20
5	244	I/O	56	63	V18	AR27	Y20
5	245	I/O	55	62	Y18	AP26	AB20
5	246	I/O	–	–	Y17	AN25	AB19
5	247	I/O	54	61	W18	AR28	AA20
–	248	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5

Table 59. EP20K200E I/O Pins (Part 9 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
–	249	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	250	I/O	–	–	AA12	AL33	AA21
4	251	I/O	51	59	AB15	AK30	Y22
4	252	I/O	–	–	AB16	AK31	AB21
4	253	I/O	–	–	AA13	AK32	U19
–	254	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	255	I/O	–	–	AB17	AL34	AB22
4	256	I/O	–	–	AA14	AM35	V19
4	257	I/O	50	58	AA15	AJ30	T18
4	258	I/O	–	–	AB18	AJ31	W21
4	259	I/O	–	57	AA16	AJ32	V20
–	260	GNDIO	GND	GND	GND	GND	GND
4	261	I/O	–	–	AB19	AJ33	V21
4	262	I/O	–	–	AB20	AK34	Y21
4	263	I/O	49	–	AA17	AL35	W22
4	264	I/O	–	55	AA18	AJ34	AA22
4	265	I/O	–	–	AB21	AH30	U20
–	266	GNDINT	GND	GND	GND	GND	GND
4	267	I/O	–	–	Y22	AH32	R17
4	268	I/O	–	–	AA20	AH33	W23
4	269	I/O	46	54	AA19	AK35	T19
4	270	I/O	–	–	V21	AH34	U21
4	271	I/O	–	–	V22	AJ35	P17
–	272	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	273	I/O	–	–	W21	AG30	R18
4	274	I/O	–	–	W22	AG31	W24
4	275	I/O	45	53	Y21	AG32	T20
4	276	I/O	–	–	W19	AG33	V24
4	277	I/O	–	–	V20	AG34	N16
–	278	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	279	I/O	–	50	Y19	AG35	V22
4	280	I/O	–	–	R17	AF30	R19
4	281	I/O	44	49	Y20	AF31	V23
4	282	I/O	–	–	T17	AF32	P18
4	283	I/O	–	–	P16	AF33	N17

Table 59. EP20K200E I/O Pins (Part 10 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
–	284	GNDIO	GND	GND	GND	GND	GND
4	285	I/O	–	–	U19	AF34	T21
4	286	I/O	–	–	T18	AF35	R21
4	287	I/O	–	48	T19	AE30	U22
4	288	I/O	–	–	V19	AE31	R20
4	289	I/O	–	–	U20	AE32	P22
–	290	GNDINT	GND	GND	GND	GND	GND
4	291	I/O	–	–	W20	AE34	N18
4	292	I/O	–	–	R18	AE35	U23
4	293	I/O	–	47	N15	AD30	N19
4	294	I/O	–	–	U21	AD31	N22
4	295	I/O	–	46	P17	AD32	L20
–	296	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	297	I/O	–	–	R19	AD33	M17
4	298	I/O	–	–	M15	AD34	T22
4	299	I/O	41	44	N16	AD35	M18
4	300	I/O	–	–	U22	AC30	T23
4	301	I/O	40	43	P18	AC31	R23
–	302	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	303	I/O	–	–	T22	AC33	U24
4	304	I/O	–	–	L14	AC34	R24
4	305	I/O	38	41	T20	AC35	T24
4	306	I/O	–	–	N17	AB30	M21
4	307	I/O	–	–	T21	AB31	M24
–	308	GNDIO	GND	GND	GND	GND	GND
4	309	I/O	–	–	M16	AB32	M22
4	310	I/O	–	–	L15	AB33	R22
4	311	I/O	37	40	P19	AB34	M23
4	312	I/O	–	–	N19	AB35	L22
4	313	I/O	–	–	R20	AA30	L21
–	314	GNDINT	GND	GND	GND	GND	GND
4	315	I/O	–	–	N18	AA32	L23
4	316	I/O	–	–	M20	AA33	L24
4	317	I/O	–	–	L16	AA34	N23
4	318	I/O	34	37	R21	AA35	AF18

Table 59. EP20K200E I/O Pins (Part 11 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
4	319	I/O	33	36	L17	Y30	AE18
–	320	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	–
4	321	I/O	–	–	L20	Y31	AF20
4	322	I/O	32	35	J18	Y32	AE20
4	323	I/O, CLK3n *(5)*	–	–	K18	Y33	M20
–	324	CLK3p	31	34	K17	Y34	M19
4	325	I/O, CLK1n *(5)*	30	–	M17	Y35	P19
–	326	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	327	nCONFIG *(7)*	29	33	M19	W32	P21
–	328	CLKLK_ENA *(11)*	28	32	M14	W33	P16
–	329	CLK1p	27	31	M18	W34	P20
–	330	MSEL1 *(7)*	26	30	L18	W35	N20
–	331	MSEL0 *(7)*	25	29	L19	U35	N21
–	332	GNDINT	GND	GND	GND	GND	GND
3	333	I/O	22	25	K15	U33	AF22
3	334	I/O	–	–	P20	U32	AE22
3	335	I/O	–	–	K16	U31	AE23
3	336	I/O	–	–	P21	T35	AF23
3	337	I/O	–	–	N21	T34	AC26
–	338	GNDIO	GND	GND	GND	GND	GND
3	339	I/O	–	–	R22	T33	AC25
3	340	I/O	–	–	N22	T32	AB25
3	341	I/O	21	24	P22	T31	AB26
3	342	I/O	–	–	K19	T30	J23
3	343	I/O	–	–	K22	R35	L19
–	344	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	345	I/O	20	23	K20	R33	AA25
3	346	I/O	–	–	N20	R32	AA26
3	347	I/O	19	22	K21	R31	L18
3	348	I/O	–	–	J20	R30	Y25
3	349	I/O	–	–	J19	P35	Y26
–	350	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	351	I/O	18	21	J21	P34	W25
3	352	I/O	–	–	J22	P33	W26

Table 59. EP20K200E I/O Pins (Part 12 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
3	353	I/O	17	20	L21	P32	J24
3	354	I/O	–	–	G21	P31	V25
3	355	I/O	–	–	J17	P30	V26
–	356	GNDINT	GND	GND	GND	GND	GND
3	357	I/O	15	18	J16	N34	U25
3	358	I/O	–	–	G22	N33	U26
3	359	I/O	14	17	H19	N32	K21
3	360	I/O	–	–	H21	N31	T25
3	361	I/O	–	–	H18	N30	T26
–	362	GNDIO	GND	GND	GND	GND	GND
3	363	I/O	–	–	H20	M35	R25
3	364	I/O	–	–	H22	M34	R26
3	365	I/O	13	16	F22	M33	K23
3	366	I/O	–	–	H17	M32	M25
3	367	I/O	–	–	G18	M31	M26
–	368	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	369	I/O	–	–	E20	L35	L25
3	370	I/O	–	–	F18	L34	L26
3	371	I/O	9	13	F20	L33	K20
3	372	I/O	–	–	G20	L32	K25
3	373	I/O	–	–	E22	L31	K26
–	374	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	375	I/O	–	–	F19	L30	J25
3	376	I/O	–	–	E19	K35	J26
3	377	I/O	7	11	G19	K34	K22
3	378	I/O	–	–	D20	K33	H25
3	379	I/O	–	–	E18	K32	H26
–	380	GNDINT	GND	GND	GND	GND	GND
3	381	I/O	–	–	D19	K30	G25
3	382	I/O	–	–	C20	J35	G26
3	383	I/O	–	10	C21	H35	K24
3	384	I/O	–	–	B20	J34	F25
3	385	I/O	–	9	D22	J33	F26
–	386	GNDIO	GND	GND	GND	GND	GND
3	387	I/O	–	–	C22	J32	E25

Table 59. EP20K200E I/O Pins (Part 13 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
3	388	I/O	–	–	F21	J31	E26
3	389	I/O	–	8	A21	J30	H24
3	390	I/O	–	–	E21	G35	D25
3	391	I/O	–	7	D21	H34	D26
–	392	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	393	I/O	–	–	A20	H33	K19
3	394	I/O	–	–	B19	H32	J20
3	395	I/O	6	4	A19	H31	G22
3	396	I/O	–	–	B18	H30	H20
3	397	I/O	–	–	A18	G34	H22
–	398	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	399	I/O	–	–	B17	E35	J22
3	400	I/O	–	–	A17	F34	G24
3	401	I/O	5	3	B16	G33	H21
3	402	I/O	–	–	A16	G32	G21
3	403	I/O	–	–	B15	G31	J21
–	404	GNDINT	GND	GND	GND	GND	GND
3	405	I/O	–	–	A15	D35	F22
3	406	I/O	–	–	B14	E34	G20
3	407	I/O	2	2	B13	F33	F21
3	408	I/O	–	–	B12	F32	E22
–	409	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2
–	410	GNDIO	GND	GND	GND	GND	GND
2	411	I/O	207	239	C19	A28	E21
2	412	I/O	–	238	D18	C25	F20
2	413	I/O	206	237	C18	B26	E20
2	414	I/O	–	–	G17	A27	J19
2	415	I/O	205	236	E17	E23	G19
2	416	I/O	–	–	D17	D23	F19
2	417	I/O	204	235	C17	C24	E19
2	418	I/O	–	–	H16	B25	K18
2	419	I/O	203	234	F16	E22	H18
2	420	I/O	202	233	E16	A26	G18
–	421	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	422	I/O	201	232	C16	C23	E18
2	423	I/O	200	231	D16	B24	F18

Table 59. EP20K200E I/O Pins (Part 14 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
2	424	I/O	198	230	C15	D22	E17
2	425	I/O	–	–	D15	A25	F17
–	426	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2
2	427	I/O	197	228	E15	E21	G17
2	428	I/O	–	–	F15	C22	H17
2	429	I/O	196	227	D14	B23	F16
2	430	I/O	195	226	G15	A24	J17
2	431	I/O	–	225	C14	A23	E16
2	432	I/O	194	224	E14	D21	G16
–	433	GNDIO	GND	GND	GND	GND	GND
2	434	I/O	193	223	F14	C21	H16
2	435	I/O	192	222	C13	E20	E15
2	436	I/O	–	221	D13	B22	F15
2	437	I/O	191	220	C12	A22	E14
2	438	I/O	–	–	F13	B21	H15
2	439	I/O	190	219	C11	A21	E13
–	440	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	–
2	441	I/O	–	–	J12	D20	L14
2	442	I/O	188	217	E13	C20	G15
2	443	I/O	–	216	H13	B20	K15
2	444	I/O	187	215	G14	A20	J16
–	445	TRST *(7)*	186	214	D12	D19	F14
–	446	NCEO *(7)*	185	213	E12	C19	G14
1	447	FAST1	184	212	F12	B19	H14
–	448	GNDINT	GND	GND	GND	GND	GND
–	449	GNDINT	–	–	–	–	–
–	450	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	451	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	452	GNDINT	GND	GND	GND	GND	GND
–	453	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	454	FAST2	181	209	D11	B17	F13
–	455	TDO *(7)*	180	208	E11	C17	G13
–	456	GNDINT	–	–	GND	GND	GND
1	457	I/O	179	207	F11	A16	H13
1	458	I/O, INITDONE *(2)*	178	206	G13	C16	J15

Table 59. EP20K200E I/O Pins (Part 15 of 15) *Note (1)*

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
1	459	I/O, RDYNBSY *(2)*	177	205	G12	A14	J14
1	460	I/O	–	–	D10	B16	F12
1	461	I/O, CLKUSR	176	204	H12	C15	K14
1	462	I/O	–	203	C10	D16	E12
1	463	I/O	175	202	C9	A15	E11
1	464	I/O	174	201	G11	B15	J13
1	465	I/O, DATA1 *(2)*	173	200	H11	C13	K13
1	466	I/O	–	–	F10	E16	H12
–	467	GNDIO	GND	GND	GND	GND	GND
–	468	VCCIO	VCCIO1	VCCIO1	–	VCCIO1	VCCIO1
1	469	I/O	171	198	C8	B14	E10
1	470	I/O	–	197	D9	D15	F11
1	471	I/O	170	196	E10	A13	G12
1	472	I/O, DATA2 *(2)*	168	195	G10	A8	J12
1	473	I/O	167	–	E9	A12	G11
1	474	I/O	166	194	C7	B13	E9
1	475	I/O	165	193	D7	C14	F9
1	476	I/O	164	192	H10	E15	K12
1	477	I/O	–	–	F9	A11	H11
1	478	I/O	–	191	C6	D14	E8
–	479	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	480	I/O	–	190	D6	B12	F8
1	481	I/O, DATA3 *(2)*	163	189	D8	B7	F10
1	482	I/O	162	187	C5	A10	E7
1	483	I/O	161	186	E8	E14	G10
1	484	I/O	–	–	F8	B11	H10
1	485	I/O, DATA4 *(2)*	160	185	E7	B5	G9
1	486	I/O	159	184	G9	C12	J11
1	487	I/O	158	183	D5	D13	F7
1	488	I/O	–	182	C4	E13	E6
1	489	I/O, DATA5 *(2)*	157	181	D4	E7	F6
–	490	GNDIO	GND	GND	GND	GND	GND

Table 60 shows configuration and power pin information for EP20K200E devices in the 208-pin RQFP, 240-pin FineLine BGA, 652-pin BGA, and 672-pin FineLine BGA packages.

Table 60. EP20K200E Configuration & Power Pins (Part 1 of 4)

Pin Name	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
MSEL0 *(7)*	25	29	L19	U35	N21
MSEL1 *(7)*	26	30	L18	W35	N20
NSTATUS *(7)*	82	92	W11	AN17	AA13
NCONFIG *(7)*)	29	33	M19	W32	P21
DCLK *(7)*	132	152	L5	U3	N7
CONF_DONE *(7)*	83	93	W10	AM17	AA12
INIT_DONE *(4)*	178	206	G13	C16	J15
nCE *(7)*	130	150	M4	U1	P6
nCEO *(7)*	185	213	E12	C19	G14
nWS *(2)*	145	164	M7	M1	P9
nRS *(2)*	142	161	L8	N1	N10
nCS *(2)*	141	160	K7	P2	M9
CS *(2)*	138	157	P4	R2	T6
RDYnBSY *(2)*	177	205	G12	A14	J14
CLKUSR *(2)*	176	204	H12	C15	K14
DATA7 *(2)*	146	166	K8	M6	M10
DATA6 *(2)*	150	169	J6	L6	L8
DATA5 *(2)*	157	181	D4	E7	F6
DATA4 *(2)*	160	185	E7	B5	G9
DATA3 *(2)*	163	189	D8	B7	F10
DATA2 *(2)*	168	195	G10	A8	J12
DATA1 *(2)*	173	200	H11	C13	K13
DATA0 *(7)*, *(8)*	133	153	L4	U4	N6
TDI *(7)*	129	149	M5	W1	P7
TDO *(7)*	180	208	E11	C17	G13
TCK *(7)*	76	87	W12	AN19	AA14
TMS *(7)*	75	86	W13	AM19	AA15
TRST *(7)*	186	214	D12	D19	F14
Dedicated Fast I/Os	77, 81, 181, 184	88, 91, 209, 212	D11, F12, V11, V12	B17, B19, AP17, AP19	F13, H13, Y13, Y14
CLK1p	27	31	M18	W34	P20
CLK2p	131	151	L6	U2	N8

Table 60. EP20K200E Configuration & Power Pins (Part 2 of 4)

Pin Name	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
CLK3p	31	34	K17	Y34	M19
CLK4p	134	154	N4	T2	R6
LOCK2 *(10)*	119	138	R4	AB6	U6
LOCK4 *(10)*	116	135	U5	AC6	W7
CLKLK_ENA *(7)*, *(11)*	28	32	M14	W33	P16
CLKLK_OUT2p	120	139	P5	Y3	T7
CLKLK_FB2p	135	155	R6	T4	U8
DEV_CLRn *(4)*	137	156	N7	T6	R9
DEV_OE *(4)*	124	143	N6	Y5	R8
VCCINT	36, 23, 11, 3, 1, 182, 156, 154, 148, 126, 121, 109, 105, 79, 52, 48	39, 27, 14, 5, 1, 210, 179, 176, 168, 145, 140, 127, 122, 90, 60, 52	B1, B22, H9, J8, J13, K11, K14 L10, M13, M22, N9, N12, P10, P15, R7, R14, AA1, AA22	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO1	172	199	G8, J10	C4, D5, E17	A6, J10, L12
VCCIO2	208,189	229	H14, K12	E19, D31, C32	A13, K16, M14
VCCIO3	8	12	J15, L13	F30, F31, U30	A21, L17, N15
VCCIO4	42	45	L22, N14, R16	W30, AL31, AL32	N24, R16, U18
VCCIO5	80,53	67	P13, T15	AN32, AN33, AL19	T15, V17, AF21
VCCIO6	86	120,97	N11, R9, T8	AL17, AM5, AN4	R13, U11, V10, AF13
VCCIO7	115	148	M10, P8	AL3, AL4, W6	P12, T10, AF6
VCCIO8	136	177	H7, K9, L1	U6, E3, E4	K9, M11, N3
VCC_CKLK2 *(3)*	125	144	L9	W4	N11
VCC_CKLK4 *(3)*	140	159	M8	R4	P10
VCC_CKOUT2 *(9)*	123	142	T5	Y1	V7

Table 60. EP20K200E Configuration & Power Pins (Part 3 of 4)

Pin Name	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
GND	43, 39, 35, 24, 16, 12, 10, 4, 199, 183, 169, 153, 149, 147, 143, 127, 118, 114, 110, 95, 78, 64, 47	175, 167, 165, 162, 146, 137, 132, 128, 108, 89, 78, 56, 51, 42, 38, 28, 26, 19, 15, 6, 240, 218, 211, 188	A1, A11, A22, B2, B21, F6, F17, G7, G16, H8, H15, J9, J11, J14, K10, K13, L2, L11, L12, M1, M11, M12, M21, N10, N13, P9, P14, R8, R15, T7, T16, U6, U17, AA2, AA21,AB1, AB11, AB22	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D17, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6, V35	A2, A8, A14, A19, A25, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N25, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19
GND_CKLK2 *(3)*	128	147	M9	W2	P11
GND_CKLK4 *(3)*	139	158	N8	R3	R10
GND_CKOUT2 *(9)*	122	141	T4	Y2	V6

Table 60. EP20K200E Configuration & Power Pins (Part 4 of 4)

Pin Name	208-Pin RQFP	240-Pin RQFP	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
No Connect (N.C.)			A9, A10, A12, A13, A14, AB9, AB10, AB12, AB13, AB14	A2, A29, A3, A30, A31, A32, A33, A34, A4, A5, A6, A7, A9, AL10, AL11, AL25, AL26, AL27, AL28, AL29, AL7, AL8, AL9, AM10, AM11, AM25, AM26, AM27, AM28, AM29, AM30, AM6 AM7, AM8, AM9, AN10, AN26, AN27, AN28, AN29, AN30, AN31, AN5, AN6, AN7, AN8, AN9, AP27, AP28, AP29, AP3, AP30, AP31, AP32, AP33, AP4, AP5, AP6, AP7, AP8, AP9, AR2, AR29, AR3, AR30, AR31, AR32, AR33 AR34, AR4, AR5, AR6, AR7, B10, B27, B28, B29, B3, B30, B31, B32, B33, B4, B6, B8, B9, C10, C11, C26, C27, C28, C29, C30, C31, C5, C6, C7, C8, C9, D10, D11, D25, D26, D27, D28, D29, D30, D6, D7, D8, D9, E10, E11, E25, E26, E27, E28, E29, E8, E9	A4, A5, A7, A9, A10, A11, A12, A15, A16, A17, A18, A20,A22, A23, B4, B5, B7, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B20, B22, B23, C5, C6, C7, C8, C9, C10, C11, C12, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, E23, E24, F23, F24, G23, H23, Y3, Y4, Y23, Y24, AA3, AA4, AA23, AA24, AB3, AB4, AB23, AB24, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AE4, AE5, AE7, AE9, AE10, AE11, AE12, AE13, AE14, AE15, AE16, AE17, AF4, AF5, AF7, AF9, AF10, AF11, AF12, AF15, AF16, AF17
Total User I/O Pins *(12)*	136	168	376	376	376

Notes to tables:

(1) For the 208-pin and 240-pin RQFP packages: Four I/O banks are supported. The VCCIO pins for I/O banks 1 and 8 combine to form a single I/O bank. The VCCIO pins for I/O banks 7 and 6 combine to form a single I/O bank. The VCCIO pins for I/O banks 5 and 4 combine to form a single I/O bank. The VCCIOs for I/O banks 3 and 2 combine to form a single I/O bank.

(2) This pin can be used as a user I/O pin after configuration.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for LVDS standard. If not used for the LVDS pair, these pins are regular I/Os. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(6) The CLKLK_OUT and CLKLK_FBIN pins are powered by the VCC_CKOUT and GND_CKOUT pins.

(7) This pin is a dedicated pin; it is not available as a user I/O pin.

(8) This pin is tri-stated in user mode.

(9) This pin is the power or ground for the external output and feedback input of a PLL. These pins should be set to the V_{CCIO} level/standard desired for the external clock output and feedback input (if used). To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the V_{CCIO} and GND_{IO} pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(10) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(11) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will begin lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(12) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Table 61 shows I/O pin information for EP20K400E devices in 652-pin BGA and 672-pin FineLine BGA packages.

Table 61. EP20K400E I/O Pins (Part 1 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
3	1	I/O	F32	E22
3	2	I/O	F33	F21
3	3	I/O	E34	G20
3	4	I/O	D35	F22
–	5	VCCINT	VCCINT	VCCINT
–	6	GNDINT	GND	GND
3	7	I/O	G31	J21
3	8	I/O	G32	G21
3	9	I/O	G33	H21
3	10	I/O	F34	G24
3	11	I/O	E35	J22
–	12	VCCIO	VCCIO3	VCCIO3
3	13	I/O	G34	H22
3	14	I/O	H30	H20
3	15	I/O	H31	G22
3	16	I/O	H32	J20
3	17	I/O	H33	K19
–	18	VCCINT	VCCINT	VCCINT
–	19	GNDINT	GND	GND
3	20	I/O, LVDSRX16p	H34	D26
3	21	I/O, LVDSRX16n *(1)*	G35	D25
3	22	I/O	J30	H24
3	23	I/O, LVDSRX15n *(1)*	J31	E26
3	24	I/O, LVDSRX15p	J32	E25
–	25	GNDIO	GND	GND
3	26	I/O, LVDSRX14p	J33	F26
3	27	I/O, LVDSRX14n *(1)*	J34	F25
3	28	I/O	H35	K24
3	29	I/O, LVDSRX13n *(1)*	J35	G26
3	30	I/O, LVDSRX13p	K30	G25
–	31	VCCINT	VCCINT	VCCINT
–	32	GNDINT	GND	GND
3	33	I/O, LVDSRX12p	K32	H26

Table 61. EP20K400E I/O Pins (Part 2 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
3	34	I/O, LVDSRX12n *(1)*	K33	H25
3	35	I/O	K34	K22
3	36	I/O, LVDSRX11n *(1)*	K35	J26
3	37	I/O, LVDSRX11p	L30	J25
–	38	VCCIO	VCCIO3	VCCIO3
3	39	I/O, LVDSRX10p	L31	K26
3	40	I/O, LVDSRX10n *(1)*	L32	K25
3	41	I/O	L33	K20
3	42	I/O, LVDSRX09n *(1)*	L34	L26
3	43	I/O, LVDSRX09p	L35	L25
–	44	VCCINT	VCCINT	VCCINT
–	45	GNDINT	GND	GND
3	46	I/O, LVDSRX08p	M31	M26
3	47	I/O, LVDSRX08n *(1)*	M32	M25
3	48	I/O	M33	K23
3	49	I/O, LVDSRX07n *(1)*	M34	R26
3	50	I/O, LVDSRX07p	M35	R25
–	51	GNDIO	GND	GND
3	52	I/O, LVDSRX06p	N30	T26
3	53	I/O, LVDSRX06n *(1)*	N31	T25
3	54	I/O	N32	K21
3	55	I/O, LVDSRX05n *(1)*	N33	U26
3	56	I/O, LVDSRX05p	N34	U25
–	57	VCCINT	VCCINT	VCCINT
–	58	GNDINT	GND	GND
3	59	I/O, LVDSRX04p	P30	V26
3	60	I/O, LVDSRX04n *(1)*	P31	V25
3	61	I/O	P32	J24
3	62	I/O, LVDSRX03n *(1)*	P33	W26
3	63	I/O, LVDSRX03p	P34	W25
–	64	VCCIO	VCCIO3	VCCIO3
3	65	I/O, LVDSRX02p	P35	Y26
3	66	I/O, LVDSRX02n *(1)*	R30	Y25
3	67	I/O, LOCK3 *(2)*	R31	L18
3	68	I/O, LVDSRX01n *(1)*	R32	AA26
3	69	I/O, LVDSRX01p	R33	AA25

Table 61. EP20K400E I/O Pins (Part 3 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	70	VCCINT	VCCINT	VCCINT
–	71	GNDINT	GND	GND
3	72	I/O	R35	L19
3	73	I/O	T30	J23
3	74	I/O, LVDSRXINCLK1n *(1)*	T31	AB26
3	75	I/O, LVDSRXINCLK1p	T32	AB25
–	76	GND_CKLK3 *(3)*	T33	AC25
–	77	GND_CKLK3 *(3)*	V35	N25
–	78	GNDIO	GND	GND
–	79	VCC_CKLK3 *(3)*	T34	AC26
3	80	I/O, CLKLK_OUT1n *(1)*	T35	AF23
–	81	CLKLK_OUT1p *(4)*	U31	AE23
–	82	GND_CKOUT1 *(5)*	U32	AE22
–	83	VCC_CKOUT1 *(5)*	U33	AF22
–	84	VCCINT	VCCINT	VCCINT
–	85	GNDINT	GND	GND
–	86	MSEL0*(6)*	U35	N21
–	87	MSEL1*(6)*	W35	N20
4	88	CLK1p	W34	P20
–	89	CLKLK_ENA *(6)*, *(7)*	W33	P16
–	90	nCONFIG *(6)*	W32	P21
–	91	VCCIO	VCCIO4	VCCIO4
–	92	GNDINT	GND	GND
–	93	VCCINT	VCCINT	VCCINT
4	94	I/O, CLK1n *(1)*	Y35	P19
4	95	CLK3p	Y34	M19
4	96	I/O, CLK3n *(1)*	Y33	M20
4	97	CLKLK_FB1p *(4)*	Y32	AE20
4	98	I/O, CLKLK_FB1n *(1)*	Y31	AF20
–	99	VCCIO	VCCIO4	VCCIO4
–	100	GND_CKLK1 *(3)*	Y30	AE18
–	101	GND_CKLK1 *(3)*	Y30	AE18
–	102	VCC_CKLK1 *(3)*	AA35	AF18
4	103	I/O	AA34	N23
4	104	I/O	AA33	L24
4	105	I/O	AA32	L23

Table 61. EP20K400E I/O Pins (Part 4 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	106	GNDINT	GND	GND
–	107	VCCINT	VCCINT	VCCINT
4	108	I/O, LOCK1 *(7)*	AA30	L21
4	109	I/O	AB35	L22
4	110	I/O	AB34	M23
4	111	I/O	AB33	R22
4	112	I/O	AB32	M22
–	113	GNDIO	GND	GND
4	114	I/O	AB31	M24
4	115	I/O	AB30	M21
4	116	I/O	AC35	T24
4	117	I/O	AC34	R24
4	118	I/O	AC33	U24
–	119	GNDINT	GND	GND
–	120	VCCINT	VCCINT	VCCINT
4	121	I/O	AC31	R23
4	122	I/O	AC30	T23
4	123	I/O	AD35	M18
4	124	I/O	AD34	T22
4	125	I/O	AD33	M17
–	126	VCCIO	VCCIO4	VCCIO4
4	127	I/O	AD32	L20
4	128	I/O	AD31	N22
4	129	I/O	AD30	N19
4	130	I/O	AE35	U23
4	131	I/O	AE34	N18
–	132	GNDINT	GND	GND
–	133	VCCINT	VCCINT	VCCINT
4	134	I/O	AE32	P22
4	135	I/O	AE31	R20
4	136	I/O	AE30	U22
4	137	I/O	AF35	R21
4	138	I/O	AF34	T21
–	139	GNDIO	GND	GND
4	140	I/O	AF33	N17
4	141	I/O	AF32	P18

Table 61. EP20K400E I/O Pins (Part 5 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
4	142	I/O	AF31	V23
4	143	I/O	AF30	R19
4	144	I/O	AG35	V22
–	145	GNDINT	GND	GND
–	146	VCCINT	VCCINT	VCCINT
4	147	I/O	AG34	N16
4	148	I/O	AG33	V24
4	149	I/O	AG32	T20
4	150	I/O	AG31	W24
4	151	I/O	AG30	R18
–	152	VCCIO	VCCIO4	VCCIO4
4	153	I/O	AJ35	P17
4	154	I/O	AH34	U21
4	155	I/O	AK35	T19
4	156	I/O	AH33	W23
4	157	I/O	AH32	R17
–	158	GNDINT	GND	GND
–	159	VCCINT	VCCINT	VCCINT
4	160	I/O	AH30	U20
4	161	I/O	AJ34	AA22
4	162	I/O	AL35	W22
4	163	I/O	AK34	Y21
4	164	I/O	AJ33	V21
–	165	GNDIO	GND	GND
4	166	I/O	AJ32	V20
4	167	I/O	AJ31	W21
4	168	I/O	AJ30	T18
4	169	I/O	AM35	V19
4	170	I/O	AL34	AB22
–	171	GNDINT	GND	GND
–	172	VCCINT	VCCINT	VCCINT
4	173	I/O	AK32	U19
4	174	I/O	AK31	AB21
4	175	I/O	AK30	Y22
4	176	I/O	AL33	AA21
–	177	VCCIO	VCCIO4	VCCIO4

Table 61. EP20K400E I/O Pins (Part 6 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	178	VCCIO	VCCIO5	VCCIO5
5	179	I/O	AL29	AB23
5	180	I/O	AM30	AA24
5	181	I/O	AP33	AA23
5	182	I/O	AN31	Y24
5	183	I/O	AR34	Y23
5	184	I/O	AP32	AC21
5	185	I/O	AL28	AC22
5	186	I/O	AM29	AB24
5	187	I/O	AN30	AA20
5	188	I/O	AR33	AD23
–	189	GNDIO	GND	GND
5	190	I/O	AP31	AC20
5	191	I/O	AL27	AB19
5	192	I/O	AR32	AB20
5	193	I/O	AM28	Y20
5	194	I/O	AN29	AC19
5	195	I/O	AP30	W20
5	196	I/O	AR31	AD22
5	197	I/O	AM27	Y19
5	198	I/O	AL26	AD21
5	199	I/O	AN28	AA19
–	200	VCCIO	VCCIO5	VCCIO5
5	201	I/O	AP29	W18
5	202	I/O	AR30	AF17
5	203	I/O	AM26	Y18
5	204	I/O	AN27	AE17
5	205	I/O	AL25	W17
5	206	I/O	AP28	AC18
5	207	I/O	AR29	AA18
5	208	I/O	AM25	AF16
5	209	I/O	AN26	Y17
5	210	I/O	AP27	AB18
–	211	GNDIO	GND	GND
–	212	GNDINT	GND	GND
–	213	GNDINT	GND	GND

Table 61. EP20K400E I/O Pins (Part 7 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	214	VCCINT	VCCINT	VCCINT
–	215	VCCINT	VCCINT	VCCINT
5	216	I/O	AR28	AD20
5	217	I/O	AN25	AA17
5	218	I/O	AP26	AE16
5	219	I/O	AR27	V16
5	220	I/O	AL23	AB17
5	221	I/O	AM23	U15
5	222	I/O	AN24	AC17
5	223	I/O	AP25	W16
5	224	I/O	AL22	AC16
5	225	I/O	AR26	Y16
–	226	VCCIO	VCCIO5	VCCIO5
5	227	I/O	AN23	AA16
5	228	I/O	AP24	AD19
5	229	I/O	AM22	T14
5	230	I/O	AR25	AB16
5	231	I/O	AL21	W15
5	232	I/O	AN22	AB15
5	233	I/O	AP23	V15
5	234	I/O	AR24	AC15
5	235	I/O	AR23	U14
5	236	I/O	AM21	AD18
–	237	GNDIO	GND	GND
5	238	I/O	AN21	AC11
5	239	I/O	AL20	Y15
5	240	I/O	AP22	AB14
5	241	I/O	AR22	V14
5	242	I/O	AP21	AB13
5	243	I/O	AR21	AD10
5	244	I/O	AM20	AC14
5	245	I/O	AN20	AC12
5	246	I/O	AP20	AD17
5	247	I/O	AR20	AC13
–	248	TMS *(6)*	AM19	AA15
–	249	TCK *(6)*	AN19	AA14

Table 61. EP20K400E I/O Pins (Part 8 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
5	250	FAST3	AP19	Y14
–	251	GNDINT	GND	GND
–	252	GNDINT	GND	GND
–	253	VCCINT	VCCINT	VCCINT
–	254	VCCINT	VCCINT	VCCINT
–	255	VCCIO	VCCIO5	VCCIO5
5	256	FAST4	AP17	Y13
–	257	nSTATUS *(6)*	AN17	AA13
–	258	CONF_DONE *(6)*	AM17	AA12
6	259	I/O	AR16	V13
6	260	I/O	AP16	AE11
6	261	I/O	AN16	W13
6	262	I/O, LVDSDESKEW	AM16	U12
6	263	I/O	AR15	U13
6	264	I/O	AP15	AF10
6	265	I/O	AR14	AB12
6	266	I/O	AP14	W14
–	267	VCCIO	VCCIO6	VCCIO6
6	268	I/O	AL16	T13
6	269	I/O	AN15	Y12
–	270	GNDIO	GND	GND
6	271	I/O	AM15	W12
6	272	I/O	AR13	AE10
6	273	I/O	AR12	V12
6	274	I/O	AP13	AF11
6	275	I/O	AN14	W11
6	276	I/O	AL15	AF9
6	277	I/O	AR11	Y11
6	278	I/O	AM14	AE9
6	279	I/O	AP12	AA11
6	280	I/O	AN13	AC10
–	281	VCCIO	VCCIO6	VCCIO6
6	282	I/O	AR10	AB10
6	283	I/O	AL14	V11
6	284	I/O	AP11	AB11
6	285	I/O	AN12	AA10

Table 61. EP20K400E I/O Pins (Part 9 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
6	286	I/O	AM13	AD9
6	287	I/O	AL13	Y10
6	288	I/O	AR9	AC9
6	289	I/O	AP10	W10
6	290	I/O	AN11	AB9
6	291	I/O	AR8	W9
–	292	GNDINT	GND	GND
–	293	GNDINT	GND	GND
–	294	VCCINT	VCCINT	VCCINT
–	295	VCCINT	VCCINT	VCCINT
–	296	GNDIO	GND	GND
6	297	I/O	AP9	Y9
6	298	I/O	AN10	AD8
6	299	I/O	AM11	Y8
6	300	I/O	AR7	AC8
6	301	I/O	AP8	AA8
6	302	I/O	AL11	AF7
6	303	I/O	AN9	AA9
6	304	I/O	AM10	AE7
6	305	I/O	AR6	T9
6	306	I/O	AP7	AD7
–	307	VCCIO	VCCIO6	VCCIO6
6	308	I/O	AN8	AC7
6	309	I/O	AL10	V8
6	310	I/O	AM9	AF5
6	311	I/O	AR5	AB8
6	312	I/O	AP6	AC6
6	313	I/O	AN7	Y7
6	314	I/O	AM8	AB7
6	315	I/O	AR4	AD6
6	316	I/O	AL9	AD5
6	317	I/O	AP5	AE5
–	318	GNDIO	GND	GND
6	319	I/O	AR3	AA3
6	320	I/O	AN6	AD4
6	321	I/O	AM7	Y3

Table 61. EP20K400E I/O Pins (Part 10 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
6	322	I/O	AL8	AF4
6	323	I/O	AP4	AB3
6	324	I/O	AR2	AE4
6	325	I/O	AN5	Y4
6	326	I/O	AP3	AC5
6	327	I/O	AM6	AA4
6	328	I/O	AL7	AB4
–	329	VCCIO	VCCIO6	VCCIO6
–	330	VCCIO	VCCIO7	VCCIO7
7	331	I/O	AK6	AB6
7	332	I/O	AK5	AA7
7	333	I/O	AK4	AA6
7	334	I/O	AK3	Y6
–	335	VCCINT	VCCINT	VCCINT
–	336	GNDINT	GND	GND
7	337	I/O	AM1	AA5
7	338	I/O	AJ6	AB5
7	339	I/O	AJ5	Y5
7	340	I/O	AJ4	W3
7	341	I/O	AJ3	V4
–	342	GNDIO	GND	GND
7	343	I/O	AK2	V5
7	344	I/O	AL1	W6
7	345	I/O	AJ2	W5
7	346	I/O	AH6	V3
7	347	I/O	AH5	U3
–	348	VCCINT	VCCINT	VCCINT
–	349	GNDINT	GND	GND
7	350	I/O, LVDSTX16p	AH3	AC2
7	351	I/O, LVDSTX16n *(1)*	AK1	AC1
7	352	I/O	AH2	W4
7	353	I/O, LVDSTX15n *(1)*	AJ1	AB2
7	354	I/O, LVDSTX15p	AG6	AB1
–	355	VCCIO	VCCIO7	VCCIO7
7	356	I/O, LVDSTX14p	AG5	AA2
7	357	I/O, LVDSTX14n *(1)*	AG4	AA1

Table 61. EP20K400E I/O Pins (Part 11 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
7	358	I/O	AG3	U4
7	359	I/O, LVDSTX13n *(1)*	AG2	Y2
7	360	I/O, LVDSTX13p	AH1	Y1
–	361	VCCINT	VCCINT	VCCINT
–	362	GNDINT	GND	GND
7	363	I/O, LVDSTX12p	AF6	W2
7	364	I/O, LVDSTX12n *(1)*	AF5	W1
7	365	I/O	AF4	T4
7	366	I/O, LVDSTX11n *(1)*	AF3	V2
7	367	I/O, LVDSTX11p	AF2	V1
–	368	GNDIO	GND	GND
7	369	I/O, LVDSTX10p	AF1	U2
7	370	I/O, LVDSTX10n *(1)*	AE6	U1
7	371	I/O	AE5	U5
7	372	I/O, LVDSTX09n *(1)*	AE4	T2
7	373	I/O, LVDSTX09p	AE3	T1
–	374	VCCINT	VCCINT	VCCINT
–	375	GNDINT	GND	GND
7	376	I/O, LVDSTX08p	AE1	R2
7	377	I/O, LVDSTX08n *(1)*	AD6	R1
7	378	I/O	AD5	T3
7	379	I/O, LVDSTX07n *(1)*	AD4	M2
7	380	I/O, LVDSTX07p	AD3	M1
–	381	VCCIO	VCCIO7	VCCIO7
7	382	I/O, LVDSTX06p	AD2	L2
7	383	I/O, LVDSTX06n *(1)*	AD1	L1
7	384	I/O, LOCK4 *(7)*	AC6	W7
7	385	I/O, LVDSTX05n *(1)*	AC5	K2
7	386	I/O, LVDSTX05p	AC4	K1
–	387	VCCINT	VCCINT	VCCINT
–	388	GNDINT	GND	GND
7	389	I/O, LVDSTX04p	AC2	J2
7	390	I/O, LVDSTX04n *(1)*	AC1	J1
7	391	I/O	AA1	T5
7	392	I/O, LVDSTX03n *(1)*	AB5	H2
7	393	I/O, LVDSTX03p	AB4	H1

Table 61. EP20K400E I/O Pins (Part 12 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	394	GNDIO	GND	GND
7	395	I/O, LVDSTX02p	AB3	G2
7	396	I/O, LVDSTX02n *(1)*	AB2	G1
7	397	I/O	AB1	R5
7	398	I/O, LVDSTX01n *(1)*	AA6	F2
7	399	I/O, LVDSTX01p	AA5	F1
–	400	VCCINT	VCCINT	VCCINT
–	401	GNDINT	GND	GND
7	402	I/O, LVDSTXOUTCLK1p	AA3	E2
7	403	I/O, LVDSTXOUTCLK1n *(1)*	AA2	E1
7	404	I/O, LOCK2 *(7)*	AB6	U6
7	405	I/O, LVDSTXINCLK1n *(1)*	Y6	D2
7	406	I/O, LVDSTXINCLK1p	W5	D1
–	407	VCCIO	VCCIO7	VCCIO7
7	408	I/O, CLKLK_OUT2n *(1)*	Y4	U7
–	409	CLKLK_OUT3p	Y3	T7
–	410	GND_CKOUT2 *(5)*	Y2	V6
–	411	VCC_CKOUT2 *(5)*	Y1	V7
7	412	I/O, DEV_OE *(8)*	Y5	R8
–	413	VCC_CKLK2 *(3)*	W4	N11
–	414	VCCINT	VCCINT	VCCINT
–	415	GNDINT	GND	GND
–	416	GND_CKLK2 *(3)*	W2	P11
–	417	GND_CKLK2 *(3)*	W2	P11
–	418	VCCIO	VCCIO7	VCCIO7
–	419	TDI *(6)*	W1	P7
–	420	nCE *(6)*	U1	P6
8	421	CLK2p	U2	N8
–	422	DCLK *(6)*	U3	N7
–	423	DATA0 *(6)*	U4	N6
–	424	GNDINT	GND	GND
–	425	VCCINT	VCCINT	VCCINT
8	426	I/O, CLK2n *(1)*	T1	N9
8	427	CLK4p	T2	R6
8	428	I/O, CLK4n *(1)*	T3	R7

Table 61. EP20K400E I/O Pins (Part 13 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
8	429	CLKLK_FB2p *(4)*	T4	U8
8	430	I/O, CLKLK_FB2n *(1)*	T5	T8
–	431	GNDIO	GND	GND
–	432	VCCIO	VCCIO8	–
8	433	I/O, DEV_CLRn *(8)*	T6	R9
8	434	I/O	R1	M4
8	435	I/O, CS *(9)*	R2	T6
–	436	GND_CKLK4 *(3)*	R3	R10
–	437	GND_CKLK4 *(3)*	R3	R10
–	438	VCC_CKLK4 *(3)*	R4	P10
–	439	GNDINT	GND	GND
–	440	VCCINT	VCCINT	VCCINT
8	441	I/O	R6	P5
8	442	I/O	P1	R3
8	443	I/O, nCS *(9)*	P2	M9
8	444	I/O	P3	P4
8	445	I/O	P4	M3
–	446	VCCIO	VCCIO8	VCCIO8
8	447	I/O	P5	M5
8	448	I/O	P6	R4
8	449	I/O, nRS *(9)*	N1	N10
8	450	I/O	N2	L3
8	451	I/O	N3	L4
–	452	GNDINT	GND	GND
–	453	VCCINT	VCCINT	VCCINT
8	454	I/O	N5	P8
8	455	I/O	N6	L5
8	456	I/O, nWS *(9)*	M1	P9
8	457	I/O	M2	M7
8	458	I/O	M3	L9
–	459	GNDIO	GND	GND
8	460	I/O	M4	L7
8	461	I/O	M5	M6
8	462	I/O, DATA7 *(9)*	M6	M10
8	463	I/O	L1	M8
8	464	I/O	L2	N5

Table 61. EP20K400E I/O Pins (Part 14 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	465	GNDINT	GND	GND
–	466	VCCINT	VCCINT	VCCINT
8	467	I/O	L4	K4
8	468	I/O	L5	K6
8	469	I/O, DATA6 *(9)*	L6	L8
8	470	I/O	K1	K8
8	471	I/O	K2	J3
–	472	VCCIO	VCCIO8	VCCIO8
8	473	I/O	K3	J7
8	474	I/O	K4	L6
8	475	I/O	K5	J6
8	476	I/O	K6	K5
8	477	I/O	J1	J4
–	478	GNDINT	GND	GND
–	479	VCCINT	VCCINT	VCCINT
8	480	I/O	J2	K3
8	481	I/O	J3	H3
8	482	I/O	J4	J8
8	483	I/O	J5	H9
8	484	I/O	J6	J5
–	485	GNDIO	GND	GND
8	486	I/O	G1	K7
8	487	I/O	H2	H6
8	488	I/O	F1	H4
8	489	I/O	H3	H7
8	490	I/O	H4	G7
–	491	GNDINT	GND	GND
–	492	VCCINT	VCCINT	VCCINT
8	493	I/O	H6	H5
8	494	I/O	G2	G6
8	495	I/O	E1	C4
8	496	I/O	F2	G4
8	497	I/O	G3	G8
–	498	VCCIO	VCCIO8	VCCIO8
8	499	I/O	G4	G3
8	500	I/O	G5	G5

Table 61. EP20K400E I/O Pins (Part 15 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
8	501	I/O	G6	D5
8	502	I/O	E2	F3
8	503	I/O	D1	E4
–	504	GNDINT	GND	GND
–	505	VCCINT	VCCINT	VCCINT
8	506	I/O	C1	F4
8	507	I/O	F4	F5
8	508	I/O	F5	E3
8	509	I/O	F6	E5
–	510	–	–	–
–	511	GNDIO	GND	GND
1	512	I/O, DATA5 *(9)*	E7	F6
1	513	I/O	D6	A4
1	514	I/O	B3	B4
1	515	I/O	C5	A5
1	516	I/O	A2	B5
1	517	I/O	B4	C6
1	518	I/O	E8	C5
1	519	I/O	D7	E6
1	520	I/O	C6	F7
1	521	I/O	A3	A7
–	522	VCCIO	VCCIO1	VCCIO1
1	523	I/O, DATA4 *(9)*	B5	G9
1	524	I/O	E9	D6
1	525	I/O	A4	D7
1	526	I/O	D8	J11
1	527	I/O	C7	B7
1	528	I/O	B6	H10
1	529	I/O	A5	C7
1	530	I/O	D9	G10
1	531	I/O	E10	E7
1	532	I/O	C8	F8
–	533	GNDIO	GND	GND
1	534	I/O, DATA3 *(9)*	B7	F10
1	535	I/O	A6	C8
1	536	I/O	D10	E8

Table 61. EP20K400E I/O Pins (Part 16 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
1	537	I/O	C9	D8
1	538	I/O	E11	H11
1	539	I/O	B8	A9
1	540	I/O	A7	K12
1	541	I/O	D11	D9
1	542	I/O	C10	F9
1	543	I/O	B9	E9
–	544	VCCIO	VCCIO1	VCCIO1
–	545	VCCINT	VCCINT	VCCINT
–	546	VCCINT	VCCINT	VCCINT
–	547	GNDINT	GND	GND
–	548	GNDINT	GND	GND
1	549	I/O, DATA2 *(9)*	A8	J12
1	550	I/O	C11	G11
1	551	I/O	B10	C9
1	552	I/O	A9	G12
1	553	I/O	E13	B9
1	554	I/O	D13	F11
1	555	I/O	C12	E10
1	556	I/O	B11	H12
–	557	VCCIO	VCCIO1	VCCIO1
1	558	I/O	E14	D10
1	559	I/O	A10	J13
–	560	GNDIO	GND	GND
1	561	I/O, DATA1 *(9)*	C13	K13
1	562	I/O	B12	C10
1	563	I/O	D14	B10
1	564	I/O	A11	E11
1	565	I/O	E15	D11
1	566	I/O	C14	D12
1	567	I/O	B13	A10
1	568	I/O	A12	E12
1	569	I/O	A13	A11
1	570	I/O	D15	F12
–	571	VCCIO	VCCIO1	VCCIO1
1	572	I/O, CLKUSR *(9)*	C15	K14

Table 61. EP20K400E I/O Pins (Part 17 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
1	573	I/O	E16	H13
1	574	I/O	B14	B12
1	575	I/O, RDYnBSY *(9)*	A14	J14
1	576	I/O	B15	B11
1	577	I/O	A15	D13
1	578	I/O	D16	A12
1	579	I/O, INITDONE *(9)*	C16	J15
1	580	I/O	B16	D14
1	581	I/O	A16	D15
–	582	GNDINT	GND	GND
–	583	TDO *(6)*	C17	G13
1	584	FAST2	B17	F13
–	585	GNDIO	GND	GND
–	586	VCCINT	VCCINT	VCCINT
–	587	VCCINT	VCCINT	VCCINT
–	588	GNDINT	GND	GND
–	589	GNDINT	GND	GND
1	590	FAST1	B19	H14
–	591	nCEO *(6)*	C19	G14
–	592	TRST *(6)*	D19	F14
2	593	I/O	A20	J16
2	594	I/O	B20	K15
2	595	I/O	C20	G15
2	596	I/O	D20	L14
2	597	I/O	A21	E13
2	598	I/O	B21	H15
2	599	I/O	A22	E14
2	600	I/O	B22	A17
2	601	I/O	E20	F15
2	602	I/O	C21	B17
–	603	VCCIO	VCCIO2	VCCIO2
2	604	I/O	D21	D16
2	605	I/O	A23	E15
2	606	I/O	A24	C17
2	607	I/O	B23	H16
2	608	I/O	C22	A18

Table 61. EP20K400E I/O Pins (Part 18 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
2	609	I/O	E21	G16
2	610	I/O	A25	E16
2	611	I/O	D22	J17
2	612	I/O	B24	D17
2	613	I/O	C23	F16
–	614	GNDIO	GND	GND
2	615	I/O	A26	H17
2	616	I/O	E22	B18
2	617	I/O	B25	G17
2	618	I/O	C24	C18
2	619	I/O	D23	F17
2	620	I/O	E23	D18
2	621	I/O	A27	E17
2	622	I/O	B26	C19
2	623	I/O	C25	F18
2	624	I/O	A28	A20
–	625	GNDINT	–	–
–	626	VCCINT	VCCINT	VCCINT
–	627	VCCINT	VCCINT	VCCINT
–	628	GNDINT	GND	GND
–	629	GNDINT	GND	GND
–	630	VCCIO	VCCIO2	VCCIO2
2	631	I/O	B27	B20
2	632	I/O	C26	E18
2	633	I/O	D25	D19
2	634	I/O	A29	G18
2	635	I/O	B28	C20
2	636	I/O	E25	H18
2	637	I/O	C27	D20
2	638	I/O	D26	K18
2	639	I/O	A30	E19
2	640	I/O	B29	F19
–	641	GNDIO	GND	GND
2	642	I/O	C28	G19
2	643	I/O	E26	A22
2	644	I/O	D27	J19

Table 61. EP20K400E I/O Pins (Part 19 of 19)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
2	645	I/O	A31	E20
2	646	I/O	B30	C21
2	647	I/O	C29	D21
2	648	I/O	D28	F20
2	649	I/O	A32	B22
2	650	I/O	E27	E21
2	651	I/O	B31	A23
–	652	VCCIO	VCCIO2	VCCIO2
2	653	I/O	A33	B23
2	654	I/O	C30	F23
2	655	I/O	D29	C22
2	656	I/O	E28	G23
2	657	I/O	B32	C23
2	658	I/O	A34	H23
2	659	I/O	C31	E24
2	660	I/O	B33	F24
2	661	I/O	D30	D22
2	662	I/O	E29	E23
–	663	GNDIO	GND	GND
–	664	VCCIO	VCCIO2	–

Table 62 shows configuration and power pin information for EP20K400E devices in 652-pin BGA and 672-pin FineLine BGA packages.

Table 62. EP20K400E Configuration & Power Pins (Part 1 of 3)

Pin Name	652-Pin BGA	672-Pin FineLine BGA
MSEL0 *(6)*	U35	N21
MSEL1 *(6)*	W35	N20
NSTATUS *(6)*	AN17	AA13
NCONFIG *(6)*	W32	P21
DCLK *(6)*	U3	N7
CONF_DONE *(6)*	AM17	AA12
INIT_DONE *(8)*	C16	J15
nCE *(6)*	U1	P6
nCEO *(6)*	C19	G14
nWS *(9)*	M1	P9
nRS *(9)*	N1	N10
nCS *(9)*	P2	M9
CS *(9)*	R2	T6
RDYnBSY *(9)*	A14	J14
CLKUSR *(9)*	C15	K14
DATA7 *(9)*	M6	M10
DATA6 *(9)*	L6	L8
DATA5 *(9)*	E7	F6
DATA4 *(9)*	B5	G9
DATA3 *(9)*	B7	F10
DATA2 *(9)*	A8	J12
DATA1 *(9)*	C13	K13
DATA0 *(6)*, *(10)*	U4	N6
TDI *(6)*	W1	P7
TDO *(6)*	C17	G13
TCK *(6)*	AN19	AA14
TMS *(6)*	AM19	AA15
TRST *(6)*	D19	F14
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14
CLK1p	W34	P20
CLK2p	U2	N8
CLK3p	Y34	M19
CLK4p	T2	R6
LOCK1 *(7)*	AA30	L21

Table 62. EP20K400E Configuration & Power Pins (Part 2 of 3)

Pin Name	652-Pin BGA	672-Pin FineLine BGA
LOCK2 *(7)*	AB6	U6
LOCK3 *(7)*	R31	L18
LOCK4 *(7)*	AC6	W7
CLKLK_ENA *(6)*, *(7)*	W33	P16
CLKLK_OUT1p	U31	AE23
CLKLK_OUT2p	Y3	T7
CLKLK_FB1p	Y32	AE20
CLKLK_FB2p	T4	U8
DEV_CLRn *(8)*	T6	R9
DEV_OE *(8)*	Y5	R8
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO1	C4, D5, E17	A6, J10, L12
VCCIO2	E19, D31, C32	A13, K16, M14
VCCIO3	F30, F31, U30	A21, L17, N15
VCCIO4	W30, AL31, AL32	N24, R16, U18
VCCIO5	AN32, AN33, AL19	T15, V17, AF21
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13
VCCIO7	AL3, AL4, W6	P12, T10, AF6
VCCIO8	U6, E3, E4	K9, M11, N3
VCC_CKLK1 *(3)*	AA35	AF18
VCC_CKLK2 *(3)*	W4	N11
VCC_CKLK3 *(3)*	T34	AC26
VCC_CKLK4 *(3)*	R4	P10
VCC_CKOUT1 *(5)*	U33	AF22
VCC_CKOUT2 *(5)*	Y1	V7

Table 62. EP20K400E Configuration & Power Pins (Part 3 of 3)

Pin Name	652-Pin BGA	672-Pin FineLine BGA
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D17, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25
GND_CKLK1 *(3)*	Y30	AE18
GND_CKLK2 *(3)*	W2	P11
GND_CKLK3 *(3)*	T33, V35	AC25, N25
GND_CKLK4 (3)	R3	R10
GND_CKOUT1 *(5)*	U32	AE22
GND_CKOUT2 *(5)*	Y2	V6
No Connect (N.C.)		A15, A16, B13, B14, B15, B16, C11, C12, C14, C15, C16, AF12, AF15, AE12, AE13, AE14, AE15, AD11, AD12, AD14, AD15, AD16
Total User I/O Pins *(11)*	488	488

Notes to tables:

(1) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for LVDS standard. If not used for the LVDS pair, these pins are regular I/Os. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(2) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) The CLKLK_OUT and CLKLK_FBIN pins are powered by the VCC_CKOUT and GND_CKOUT pins.

(5) This pin is the power or ground for the external output and feedback input of a PLL. These pins should be set to the V_{CCIO} level/standard desired for the external clock output and feedback input (if used). To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the V_{CCIO} and GND_{IO} pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will begin lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(8) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(9) This pin can be used as a user I/O pin after configuration.

(10) This pin is tri-stated in user mode.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Table 63 shows I/O pin information for EP20K600E devices in 652-pin BGA, 672-pin FineLine BGA, and 1,020-pin FineLine BGA packages.

Table 63. EP20K600E I/O Pins (Part 1 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	1	I/O	–	H23	B28
2	2	I/O	–	E24	C29
–	3	VCCINT	VCCINT	VCCINT	VCCINT
–	4	GNDINT	GND	GND	GND
2	5	I/O	–	F24	C28
2	6	I/O	–	D22	D30
2	7	I/O	–	E23	D29
–	8	VCCIO	VCCIO2	VCCIO2	VCCIO2
–	9	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	10	I/O	–	–	D28
3	11	I/O	F32	E22	E30
3	12	I/O	–	–	E29
3	13	I/O	F33	F21	E28
–	14	VCCINT	VCCINT	VCCINT	VCCINT
–	15	GNDINT	GND	GND	GND
3	16	I/O	–	–	F28
3	17	I/O	–	–	G28
3	18	I/O	E34	G20	G27
3	19	I/O	–	–	H29
3	20	I/O	D35	F22	H28
–	21	GNDIO	GND	GND	GND
3	22	I/O	–	–	H27
3	23	I/O	–	–	H26
3	24	I/O	G31	J21	J29
3	25	I/O	–	–	J28
3	26	I/O	G32	G21	J27
–	27	VCCINT	VCCINT	VCCINT	VCCINT
–	28	GNDINT	GND	GND	GND
3	29	I/O	–	–	J26
3	30	I/O	–	–	K29
3	31	I/O	G33	H21	K28
3	32	I/O	–	–	K27

Table 63. EP20K600E I/O Pins (Part 2 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	33	I/O	F34	G24	K26
–	34	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	35	I/O	–	–	L28
3	36	I/O	–	–	L27
3	37	I/O	E35	J22	L26
3	38	I/O	–	–	M28
3	39	I/O	G34	H22	M27
–	40	VCCINT	VCCINT	VCCINT	VCCINT
–	41	GNDINT	GND	GND	GND
3	42	I/O	–	–	M26
3	43	I/O	–	–	M25
3	44	I/O	H30	H20	M23
3	45	I/O	–	–	M22
3	46	I/O	H31	G22	N29
–	47	GNDIO	GND	GND	GND
3	48	I/O	–	–	N28
3	49	I/O	–	–	N27
3	50	I/O	H32	J20	N26
3	51	I/O	–	–	N25
3	52	I/O	H33	K19	N23
–	53	VCCINT	VCCINT	VCCINT	VCCINT
–	54	GNDINT	GND	GND	GND
3	55	I/O, LVDSRX16p	H34	D26	D31
3	56	I/O, LVDSRX16n *(1)*	G35	D25	D32
3	57	I/O	J30	H24	N22
3	58	I/O, LVDSRX15n *(1)*	J31	E26	E31
3	59	I/O, LVDSRX15p	J32	E25	E32
–	60	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	61	I/O, LVDSIN14p	J33	F26	H31
3	62	I/O, LVDSIN 14n *(1)*	J34	F25	H32
3	63	I/O	H35	K24	P29
3	64	I/O, LVDSRX13n *(1)*	J35	G26	J31
3	65	I/O, LVDSRX13p	K30	G25	J32
–	66	VCCINT	VCCINT	VCCINT	VCCINT
–	67	GNDINT	GND	GND	GND

Table 63. EP20K600E I/O Pins (Part 3 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	68	I/O, LVDSRX12p	K32	H26	K31
3	69	I/O, LVDSRX12n *(1)*	K33	H25	K32
3	70	I/O	K34	K22	P28
3	71	I/O, LVDSRX11n *(1)*	K35	J26	N31
3	72	I/O, LVDSRX11p	L30	J25	N32
–	73	GNDIO	GND	GND	GND
3	74	I/O, LVDSRX10p	L31	K26	P31
3	75	I/O, LVDSRX10n *(1)*	L32	K25	P32
3	76	I/O	L33	K20	P27
3	77	I/O, LVDSRX09n *(1)*	L34	L26	R31
3	78	I/O, LVDSRX09p	L35	L25	R32
–	79	VCCINT	VCCINT	VCCINT	VCCINT
–	80	GNDINT	GND	GND	GND
3	81	I/O, LVDSRX08p	M31	M26	V31
3	82	I/O, LVDSRX08n *(1)*	M32	M25	V32
3	83	I/O	M33	K23	P26
3	84	I/O, LVDSRX07n *(1)*	M34	R26	W31
3	85	I/O, LVDSRX07p	M35	R25	W32
–	86	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	87	I/O, LVDSRX06p	N30	T26	Y31
3	88	I/O, LVDSRX06n	N31	T25	Y32
3	89	I/O	N32	K21	P25
3	90	I/O, LVDSRX05n *(1)*	N33	U26	AC31
3	91	I/O, LVDSRX05p	N34	U25	AC32
–	92	VCCINT	VCCINT	VCCINT	VCCINT
–	93	GNDINT	GND	GND	GND
3	94	I/O, LVDSRX04p	P30	V26	AD31
3	95	I/O, LVDSRX04n *(1)*	P31	V25	AD32
3	96	I/O	P32	J24	P22
3	97	I/O, LVDSRX03n *(1)*	P33	W26	AE31
3	98	I/O, LVDSRX03p	P34	W25	AE32
–	99	GNDIO	GND	GND	GND
3	100	I/O, LVDSRX02p	P35	Y26	AH31
3	101	I/O, LVDSRX02n *(1)*	R30	Y25	AH32
3	102	I/O, LOCK3 *(2)*	R31	L18	H30

Table 63. EP20K600E I/O Pins (Part 4 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	103	I/O, LVDSRX01n *(1)*	R32	AA26	AJ31
3	104	I/O, LVDSRX01p	R33	AA25	AJ32
–	105	VCCINT	VCCINT	VCCINT	VCCINT
–	106	GNDINT	GND	GND	GND
3	107	I/O	R35	L19	R29
3	108	I/O	T30	J23	R28
3	109	I/O, LVDSRXINCLK1n	T31	AB26	A29
3	110	I/O, LVDSRXINCLK1p	T32	AB25	B29
–	111	GND_CKLK3 *(3)*	T33	AC25	P24
–	112	GND_CKLK3 *(3)*	V35	N25	P23
–	113	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	114	VCC_CKLK3 *(3)*	T34	AC26	M24
3	115	I/O, CLKLK_OUT1n *(1)*	T35	AF23	AL29
–	116	CLKLK_OUT1p	U31	AE23	AM29
–	117	GND_CKOUT1 *(4)*	U32	AE22	T24
–	118	VCC_CKOUT1 *(4)*	U33	AF22	N24
–	119	VCCINT	VCCINT	VCCINT	VCCINT
–	120	GNDINT	GND	GND	GND
–	121	MSEL0 *(5)*	U35	N21	J30
–	122	MSEL1 *(5)*	W35	N20	K30
4	123	CLK1p	W34	P20	N30
–	124	CLKLK_ENA *(5)*, *(6)*	W33	P16	P30
–	125	nCONFIG *(5)*	W32	P21	R30
–	126	GNDINT	GND	GND	GND
–	127	VCCINT	VCCINT	VCCINT	VCCINT
4	128	I/O, CLK1n *(1)*	Y35	P19	V30
4	129	CLK3p	Y34	M19	W30
4	130	I/O, CLK3n *(1)*	Y33	M20	Y30
4	131	CLKLK_FB1p	Y32	AE20	AL28
4	132	I/O, CLKLK_FB1n *(1)*	Y31	AF20	AM28
–	133	GNDIO	GND	GND	GND
–	134	GND_CKLK1 *(3)*	Y30	AE18	V24
–	135	GND_CKLK1 *(3)*	Y30	AE18	V24
–	136	VCC_CKLK1 *(3)*	AA35	AF18	W24
4	137	I/O	AA34	N23	R27

Table 63. EP20K600E I/O Pins (Part 5 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	138	I/O	AA33	L24	R26
4	139	I/O	AA32	L23	R25
–	140	GNDINT	GND	GND	GND
–	141	VCCINT	VCCINT	VCCINT	VCCINT
4	142	I/O, LOCK1 *(2)*	AA30	L21	AC30
4	143	I/O	AB35	L22	R24
4	144	I/O	AB34	M23	R23
4	145	I/O	AB33	R22	R22
4	146	I/O	AB32	M22	T29
–	147	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	148	I/O	AB31	M24	T28
4	149	I/O	AB30	M21	T27
4	150	I/O	AC35	T24	T26
4	151	I/O	AC34	R24	T25
4	152	I/O	AC33	U24	T23
–	153	GNDINT	GND	GND	GND
–	154	VCCINT	VCCINT	VCCINT	VCCINT
4	155	I/O	AC31	R23	T22
4	156	I/O	AC30	T23	U29
4	157	I/O	AD35	M18	U28
4	158	I/O	AD34	T22	U27
4	159	I/O	AD33	M17	U26
–	160	GNDIO	GND	GND	GND
4	161	I/O	AD32	L20	U25
4	162	I/O	AD31	N22	U24
4	163	I/O	AD30	N19	U23
4	164	I/O	AE35	U23	U22
4	165	I/O	AE34	N18	V29
–	166	GNDINT	GND	GND	GND
–	167	VCCINT	VCCINT	VCCINT	VCCINT
4	168	I/O	AE32	P22	V28
4	169	I/O	AE31	R20	V27
4	170	I/O	AE30	U22	V26
4	171	I/O	AF35	R21	V25
4	172	I/O	AF34	T21	V23

Table 63. EP20K600E I/O Pins (Part 6 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	173	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	174	I/O	AF33	N17	V22
4	175	I/O	AF32	P18	W29
4	176	I/O	AF31	V23	W28
4	177	I/O	AF30	R19	W27
4	178	I/O	AG35	V22	W26
–	179	GNDINT	GND	GND	GND
–	180	VCCINT	VCCINT	VCCINT	VCCINT
4	181	I/O	AG34	N16	W25
4	182	I/O	AG33	V24	W23
4	183	I/O	AG32	T20	W22
4	184	I/O	AG31	W24	Y29
4	185	I/O	AG30	R18	Y28
–	186	GNDIO	GND	GND	GND
4	187	I/O	AJ35	P17	Y27
4	188	I/O	AH34	U21	Y26
4	189	I/O	AK35	T19	Y25
4	190	I/O	AH33	W23	Y24
4	191	I/O	AH32	R17	Y23
–	192	GNDINT	GND	GND	GND
–	193	VCCINT	VCCINT	VCCINT	VCCINT
4	194	I/O	AH30	U20	Y22
4	195	I/O	–	–	AA28
4	196	I/O	AJ34	AA22	AA27
4	197	I/O	–	–	AA26
4	198	I/O	–	–	AA25
–	199	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	200	I/O	AL35	W22	AA24
4	201	I/O	–	–	AA23
4	202	I/O	AK34	Y21	AA22
4	203	I/O	–	–	AB28
4	204	I/O	–	–	AB27
–	205	GNDINT	GND	GND	GND
–	206	VCCINT	VCCINT	VCCINT	VCCINT
4	207	I/O	AJ33	V21	AB26

Table 63. EP20K600E I/O Pins (Part 7 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	208	I/O	–	–	AC29
4	209	I/O	AJ32	V20	AC28
4	210	I/O	–	–	AC27
4	211	I/O	–	–	AC26
–	212	GNDIO	GND	GND	GND
4	213	I/O	AJ31	W21	AD30
4	214	I/O	–	–	AD29
4	215	I/O	AJ30	T18	AD28
4	216	I/O	–	–	AD27
4	217	I/O	–	–	AD26
–	218	GNDINT	GND	GND	GND
–	219	VCCINT	VCCINT	VCCINT	VCCINT
4	220	I/O	AM35	V19	AE30
4	221	I/O	–	–	AE29
4	222	I/O	AL34	AB22	AE28
4	223	I/O	–	–	AE27
4	224	I/O	–	–	AE26
–	225	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	226	I/O	AK32	U19	AF28
4	227	I/O	–	–	AF27
4	228	I/O	AK31	AB21	AG28
4	229	I/O	–	–	AG27
4	230	I/O	–	–	AH30
–	231	GNDINT	GND	GND	GND
–	232	VCCINT	VCCINT	VCCINT	VCCINT
4	233	I/O	AK30	Y22	AH29
4	234	I/O	–	–	AH28
4	235	I/O	AL33	AA21	AJ30
4	236	I/O	–	–	AJ29
–	237	GNDIO	GND	GND	GND
5	238	I/O	–	AB23	AJ28
5	239	I/O	–	AA24	AK29
5	240	I/O	–	AA23	AK28
–	241	GNDINT	GND	GND	GND
–	242	VCCINT	VCCINT	VCCINT	VCCINT

Table 63. EP20K600E I/O Pins (Part 8 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	243	I/O	–	Y24	AH27
5	244	I/O	–	Y23	AF26
–	245	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	246	I/O	AL29	AC21	AG26
5	247	I/O	AM30	AC22	AH26
5	248	I/O	AP33	AB24	AE25
5	249	I/O	AN31	AA20	AF25
5	250	I/O	AR34	AD23	AG25
5	251	I/O	AP32	AC20	AH25
5	252	I/O	AL28	AB19	AJ25
5	253	I/O	AM29	AB20	AK25
5	254	I/O	AN30	Y20	AL25
5	255	I/O	AR33	AC19	AM25
–	256	GNDIO	GND	GND	GND
5	257	I/O	AP31	W20	AE24
5	258	I/O	AL27	AD22	AF24
5	259	I/O	AR32	Y19	AG24
5	260	I/O	AM28	AD21	AH24
5	261	I/O	AN29	AA19	AJ24
5	262	I/O	AP30	W18	AK24
5	263	I/O	AR31	AF17	AL24
5	264	I/O	AM27	Y18	AM24
5	265	I/O	AL26	AE17	AE23
5	266	I/O	AN28	W17	AF23
–	267	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	268	I/O	AP29	AC18	AG23
5	269	I/O	AR30	AA18	AH23
5	270	I/O	AM26	AF16	AJ23
5	271	I/O	AN27	Y17	AK23
5	272	I/O	AL25	AB18	AL23
5	273	I/O	AP28	AD20	AM23
5	274	I/O	AR29	AA17	AE22
5	275	I/O	AM25	AE16	AF22
5	276	I/O	AN26	V16	AG22
5	277	I/O	AP27	AB17	AH22

Table 63. EP20K600E I/O Pins (Part 9 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	278	GNDIO	GND	GND	GND
–	279	GNDINT	GND	GND	GND
–	280	GNDINT	GND	GND	GND
–	281	VCCINT	VCCINT	VCCINT	VCCINT
–	282	VCCINT	VCCINT	VCCINT	VCCINT
5	283	I/O	AR28	U15	AE21
5	284	I/O	AN25	AC17	AF21
5	285	I/O	AP26	W16	AG21
5	286	I/O	AR27	AC16	AH21
5	287	I/O	AL23	Y16	AE20
5	288	I/O	AM23	AA16	AF20
5	289	I/O	AN24	AD19	AG20
5	290	I/O	AP25	T14	AH20
5	291	I/O	AL22	AB16	AJ20
5	292	I/O	AR26	W15	AK20
–	293	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	294	I/O	AN23	AB15	AL20
5	295	I/O	AP24	V15	AF19
5	296	I/O	AM22	AC15	AG19
5	297	I/O	AR25	U14	AH19
5	298	I/O	AL21	AD18	AJ19
5	299	I/O	AN22	AC11	AK19
5	300	I/O	AP23	Y15	AL19
5	301	I/O	AR24	AB14	AF18
5	302	I/O	AR23	V14	AG18
5	303	I/O	AM21	AB13	AH18
–	304	GNDIO	GND	GND	GND
5	305	I/O	AN21	AD10	AJ18
5	306	I/O	AL20	AC14	AK18
5	307	I/O	AP22	AC12	AL18
5	308	I/O	AR22	AD17	AF17
5	309	I/O	AP21	AC13	AG17
5	310	I/O	AR21	AD16	AH17
5	311	I/O	AM20	AD15	AJ17
5	312	I/O	AN20	AE15	AK17

Table 63. EP20K600E I/O Pins (Part 10 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	313	I/O	AP20	AD14	AK16
5	314	I/O	AR20	AE14	AJ16
–	315	TMS *(5)*	AM19	AA15	AM20
–	316	TCK *(5)*	AN19	AA14	AM19
5	317	FAST3	AP19	Y14	AM18
–	318	GNDINT	GND	GND	GND
–	319	GNDINT	GND	GND	GND
–	320	VCCINT	VCCINT	VCCINT	VCCINT
–	321	VCCINT	VCCINT	VCCINT	VCCINT
–	322	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	323	FAST4	AP17	Y13	AM15
–	324	nSTATUS *(5)*	AN17	AA13	AM14
–	325	CONF_DONE *(5)*	AM17	AA12	AM13
–	326	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	327	I/O	AR16	AE13	AH16
6	328	I/O	AP16	AF12	AG16
6	329	I/O	AN16	AE12	AF16
6	330	I/O, LVDSDESKEW	AM16	U12	AM10
6	331	I/O	AR15	AD12	AL15
6	332	I/O	AP15	AD11	AK15
6	333	I/O	AR14	V13	AJ15
6	334	I/O	AP14	AE11	AH15
6	335	I/O	AL16	W13	AG15
6	336	I/O	AN15	U13	AF15
–	337	GNDIO	GND	GND	GND
6	338	I/O	AM15	AF10	AL14
6	339	I/O	AR13	AB12	AK14
6	340	I/O	AR12	W14	AJ14
6	341	I/O	AP13	T13	AH14
6	342	I/O	AN14	Y12	AG14
6	343	I/O	AL15	W12	AF14
6	344	I/O	AR11	AE10	AL13
6	345	I/O	AM14	V12	AK13
6	346	I/O	AP12	AF11	AJ13
6	347	I/O	AN13	W11	AH13

Table 63. EP20K600E I/O Pins (Part 11 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	348	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	349	I/O	AR10	AF9	AG13
6	350	I/O	AL14	Y11	AF13
6	351	I/O	AP11	AE9	AE13
6	352	I/O	AN12	AA11	AH12
6	353	I/O	AM13	AC10	AG12
6	354	I/O	AL13	AB10	AF12
6	355	I/O	AR9	V11	AE12
6	356	I/O	AP10	AB11	AH11
6	357	I/O	AN11	AA10	AG11
6	358	I/O	AR8	AD9	AF11
–	359	GNDINT	GND	GND	GND
–	360	GNDINT	GND	GND	GND
–	361	VCCINT	VCCINT	VCCINT	VCCINT
–	362	VCCINT	VCCINT	VCCINT	VCCINT
–	363	GNDIO	GND	GND	GND
6	364	I/O	AP9	Y10	AE11
6	365	I/O	AN10	AC9	AL10
6	366	I/O	AM11	W10	AK10
6	367	I/O	AR7	AB9	AJ10
6	368	I/O	AP8	W9	AH10
6	369	I/O	AL11	Y9	AG10
6	370	I/O	AN9	AD8	AF10
6	371	I/O	AM10	Y8	AE10
6	372	I/O	AR6	AC8	AM9
6	373	I/O	AP7	AA8	AL9
–	374	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	375	I/O	AN8	AF7	AK9
6	376	I/O	AL10	AA9	AJ9
6	377	I/O	AM9	AE7	AH9
6	378	I/O	AR5	T9	AG9
6	379	I/O	AP6	AD7	AF9
6	380	I/O	AN7	AC7	AE9
6	381	I/O	AM8	V8	AM8
6	382	I/O	AR4	AF5	AL8

Table 63. EP20K600E I/O Pins (Part 12 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
6	383	I/O	AL9	AB8	AK8
6	384	I/O	AP5	AC6	AJ8
–	385	GNDIO	GND	GND	GND
6	386	I/O	AR3	Y7	AH8
6	387	I/O	AN6	AB7	AG8
6	388	I/O	AM7	AD6	AF8
6	389	I/O	AL8	AD5	AE8
6	390	I/O	AP4	AE5	AH7
6	391	I/O	AR2	AA3	AG7
6	392	I/O	AN5	AD4	AF7
6	393	I/O	AP3	Y3	AH6
6	394	I/O	AM6	AF4	AJ5
6	395	I/O	AL7	AB3	AJ4
–	396	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	397	I/O	–	AE4	AH5
6	398	I/O	–	Y4	AH4
–	399	VCCINT	VCCINT	VCCINT	VCCINT
–	400	GNDINT	GND	GND	GND
6	401	I/O	–	AC5	AG6
6	402	I/O	–	AA4	AG5
6	403	I/O	–	AB4	AF6
–	404	GNDIO	GND	GND	GND
7	405	I/O	–	–	AF5
7	406	I/O	AK6	AB6	AE7
7	407	I/O	–	–	AE6
7	408	I/O	AK5	AA7	AE5
–	409	VCCINT	VCCINT	VCCINT	VCCINT
–	410	GNDINT	GND	GND	GND
7	411	I/O	–	–	AE4
7	412	I/O	–	–	AD7
7	413	I/O	AK4	AA6	AD6
7	414	I/O	–	–	AD5
7	415	I/O	AK3	Y6	AD4
–	416	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	417	I/O	–	–	AC7

Table 63. EP20K600E I/O Pins (Part 13 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	418	I/O	–	–	AC6
7	419	I/O	AM1	AA5	AC5
7	420	I/O	–	–	AC4
7	421	I/O	AJ6	AB5	AB7
–	422	VCCINT	VCCINT	VCCINT	VCCINT
–	423	GNDINT	GND	GND	GND
7	424	I/O	–	–	AB6
7	425	I/O	–	–	AB5
7	426	I/O	AJ5	Y5	AA11
7	427	I/O	–	–	AA10
7	428	I/O	AJ4	W3	AA8
–	429	GNDIO	GND	GND	GND
7	430	I/O	–	–	AA7
7	431	I/O	–	–	AA6
7	432	I/O	AJ3	V4	AA5
7	433	I/O	–	–	Y11
7	434	I/O	AK2	V5	Y10
–	435	VCCINT	VCCINT	VCCINT	VCCINT
–	436	GNDINT	GND	GND	GND
7	437	I/O	–	–	Y8
7	438	I/O	–	–	Y7
7	439	I/O	AL1	W6	Y6
7	440	I/O	–	–	Y5
7	441	I/O	AJ2	W5	Y4
–	442	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	443	I/O	–	–	W11
7	444	I/O	–	–	W10
7	445	I/O	AH6	V3	W8
7	446	I/O	–	–	W7
7	447	I/O	AH5	U3	W6
–	448	VCCINT	VCCINT	VCCINT	VCCINT
–	449	GNDINT	GND	GND	GND
7	450	I/O, LVDSTX16p	AH3	AC2	AJ2
7	451	I/O, LVDSTX16n *(1)*	AK1	AC1	AJ1
7	452	I/O	AH2	W4	W5

Table 63. EP20K600E I/O Pins (Part 14 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	453	I/O, LVDSTX15n *(1)*	AJ1	AB2	AH2
7	454	I/O, LVDSTX15p	AG6	AB1	AH1
–	455	GNDIO	GND	GND	GND
7	456	I/O, LVDSTX14p	AG5	AA2	AE2
7	457	I/O, LVDSTX14n *(1)*	AG4	AA1	AE1
7	458	I/O	AG3	U4	W4
7	459	I/O, LVDSTX13n *(1)*	AG2	Y2	AD2
7	460	I/O, LVDSTX13p	AH1	Y1	AD1
–	461	VCCINT	VCCINT	VCCINT	VCCINT
–	462	GNDINT	GND	GND	GND
7	463	I/O, LVDSTX12p	AF6	W2	AC2
7	464	I/O, LVDSTX12n *(1)*	AF5	W1	AC1
7	465	I/O	AF4	T4	V11
7	466	I/O, LVDSTX11n *(1)*	AF3	V2	Y2
7	467	I/O, LVDSTX11p	AF2	V1	Y1
–	468	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	469	I/O, LVDSTX10p	AF1	U2	W2
7	470	I/O, LVDSTX10n *(1)*	AE6	U1	W1
7	471	I/O	AE5	U5	V10
7	472	I/O, LVDSTX09n *(1)*	AE4	T2	V2
7	473	I/O, LVDSTX09p	AE3	T1	V1
–	474	VCCINT	VCCINT	VCCINT	VCCINT
–	475	GNDINT	GND	GND	GND
7	476	I/O, LVDSTX08p	AE1	R2	R2
7	477	I/O, LVDSTX08n *(1)*	AD6	R1	R1
7	478	I/O	AD5	T3	V8
7	479	I/O, LVDSTX07n *(1)*	AD4	M2	P2
7	480	I/O, LVDSTX07p	AD3	M1	P1
–	481	GNDIO	GND	GND	GND
7	482	I/O, LVDSTX06p	AD2	L2	N2
7	483	I/O, LVDSTX06n *(1)*	AD1	L1	N1
7	484	I/O, LOCK4 *(2)*	AC6	W7	AK5
7	485	I/O, LVDSTX05n *(1)*	AC5	K2	K2
7	486	I/O, LVDSTX05p	AC4	K1	K1
–	487	VCCINT	VCCINT	VCCINT	VCCINT

Table 63. EP20K600E I/O Pins (Part 15 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	488	GNDINT	GND	GND	GND
7	489	I/O, LVDSTX04p	AC2	J2	J2
7	490	I/O, LVDSTX04n *(1)*	AC1	J1	J1
7	491	I/O	AB1	T5	V7
7	492	I/O, LVDSTX03n *(1)*	AB5	H2	H2
7	493	I/O, LVDSTX03p	AB4	H1	H1
–	494	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	495	I/O, LVDSTX02p	AB3	G2	E2
7	496	I/O, LVDSTX02n *(1)*	AB2	G1	E1
7	497	I/O	AA1	R5	V6
7	498	I/O, LVDSTX01n *(1)*	AA6	F2	D2
7	499	I/O, LVDSTX01p	AA5	F1	D1
–	500	VCCINT	VCCINT	VCCINT	VCCINT
–	501	GNDINT	GND	GND	GND
7	502	I/O, LVDSTXOUTCLK1p	AA3	E2	AL4
7	503	I/O, LVDSTXOUTCLK1n *(1)*	AA2	E1	AM4
7	504	I/O, LOCK2 *(2)*	AB6	U6	AK4
7	505	I/O, CLK_LVDSTXINCLK1p	Y6	D2	AL5
7	506	I/O, LVDSTXINCLK1p	W5	D1	AM5
–	507	GNDIO	GND	GND	GND
7	508	I/O, CLKLK_OUT2n *(1)*	Y4	U7	AJ3
–	509	CLKLK_OUT2p	Y3	T7	AH3
–	510	GND_CKOUT2 *(4)*	Y2	V6	W9
–	511	VCC_CKOUT2 *(4)*	Y1	V7	AA9
7	512	I/O, DEV_OE *(7)*	Y5	R8	AE3
–	513	VCC_CKLK2 *(3)*	W4	N11	Y9
–	514	VCCINT	VCCINT	VCCINT	VCCINT
–	515	GNDINT	GND	GND	GND
–	516	GND_CKLK2 *(3)*	W2	P11	V9
–	517	GND_CKLK2 *(3)*	W2	P11	V9
–	518	TDI *(5)*	W1	P7	AD3

Table 63. EP20K600E I/O Pins (Part 16 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	519	nCE *(5)*	U1	P6	AC3
8	520	CLK2p	U2	N8	Y3
–	521	DCLK *(5)*	U3	N7	W3
–	522	DATA0 *(5)*	U4	N6	V3
–	523	GNDINT	GND	GND	GND
–	524	VCCINT	VCCINT	VCCINT	VCCINT
8	525	I/O, CLK2n *(1)*	T1	N9	R3
8	526	CLK4p	T2	R6	P3
8	527	I/O, CLK4n *(1)*	T3	R7	N3
8	528	CLKLK_FB2p	T4	U8	K3
8	529	I/O, CLKLK_FB2n *(1)*	T5	T8	J3
–	530	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	531	I/O, DEV_CLRn *(7)*	T6	R9	H3
8	532	I/O	R1	M4	V5
8	533	I/O, CS *(8)*	R2	T6	E3
–	534	GND_CKLK4 *(3)*	R3	R10	T9
–	535	GND_CKLK4 *(3)*	R3	R10	T9
–	536	VCC_CKLK4 *(3)*	R4	P10	P9
–	537	GNDINT	GND	GND	GND
–	538	VCCINT	VCCINT	VCCINT	VCCINT
8	539	I/O	R6	P5	V4
8	540	I/O	P1	R3	U11
8	541	I/O, nCS *(8)*	P2	M9	D3
8	542	I/O	P3	P4	U10
8	543	I/O	P4	M3	U9
–	544	GNDIO	GND	GND	GND
8	545	I/O	P5	M5	U8
8	546	I/O	P6	R4	U7
8	547	I/O, nRS *(8)*	N1	N10	D4
8	548	I/O	N2	L3	U6
8	549	I/O	N3	L4	U5
–	550	GNDINT	GND	GND	GND
–	551	VCCINT	VCCINT	VCCINT	VCCINT
8	552	I/O	N5	P8	U4
8	553	I/O	N6	L5	T11

Table 63. EP20K600E I/O Pins (Part 17 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	554	I/O, nWS *(8)*	M1	P9	C4
8	555	I/O	M2	M7	T10
8	556	I/O	M3	L9	T8
–	557	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	558	I/O	M4	L7	T7
8	559	I/O	M5	M6	T6
8	560	I/O, DATA7 *(8)*	M6	M10	B4
8	561	I/O	L1	M8	T5
8	562	I/O	L2	N5	T4
–	563	GNDINT	GND	GND	GND
–	564	VCCINT	VCCINT	VCCINT	VCCINT
8	565	I/O	L4	K4	R11
8	566	I/O	L5	K6	R9
8	567	I/O, DATA6 *(8)*	L6	L8	A4
8	568	I/O	K1	K8	R10
8	569	I/O	K2	J3	R8
–	570	GNDIO	GND	GND	GND
8	571	I/O	K3	J7	R7
8	572	I/O	K4	L6	R6
8	573	I/O	K5	J6	R5
8	574	I/O	K6	K5	R4
8	575	I/O	J1	J4	P11
–	576	GNDINT	GND	GND	GND
–	577	VCCINT	VCCINT	VCCINT	VCCINT
8	578	I/O	J2	K3	P10
8	579	I/O	J3	H3	P8
8	580	I/O	J4	J8	P7
8	581	I/O	J5	H9	P6
8	582	I/O	J6	J5	P5
–	583	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	584	I/O	G1	K7	P4
8	585	I/O	H2	H6	N11
8	586	I/O	F1	H4	N10
8	587	I/O	H3	H7	N9
8	588	I/O	H4	G7	N8

Table 63. EP20K600E I/O Pins (Part 18 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	589	GNDINT	GND	GND	GND
–	590	VCCINT	VCCINT	VCCINT	VCCINT
8	591	I/O	H6	H5	N7
8	592	I/O	–	–	N6
8	593	I/O	G2	G6	N5
8	594	I/O	–	–	N4
8	595	I/O	–	–	M11
–	596	GNDIO	GND	GND	GND
8	597	I/O	E1	C4	M10
8	598	I/O	–	–	M9
8	599	I/O	F2	G4	M8
8	600	I/O	–	–	M7
8	601	I/O	–	–	M6
–	602	GNDINT	GND	GND	GND
–	603	VCCINT	VCCINT	VCCINT	VCCINT
8	604	I/O	G3	G8	M5
8	605	I/O	–	–	L8
8	606	I/O	G4	G3	L7
8	607	I/O	–	–	L6
8	608	I/O	–	–	L5
–	609	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	610	I/O	G5	G5	K8
8	611	I/O	–	–	K7
8	612	I/O	G6	D5	K6
8	613	I/O	–	–	K5
8	614	I/O	–	–	K4
–	615	GNDINT	GND	GND	GND
–	616	VCCINT	VCCINT	VCCINT	VCCINT
8	617	I/O	E2	F3	J8
8	618	I/O	–	–	J7
8	619	I/O	D1	E4	J6
8	620	I/O	–	–	J5
8	621	I/O	–	–	J4
–	622	GNDIO	GND	GND	GND
8	623	I/O	C1	F4	H7

Table 63. EP20K600E I/O Pins (Part 19 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	624	I/O	–	–	H6
8	625	I/O	F4	F5	H5
8	626	I/O	–	–	H4
8	627	I/O	–	–	G7
–	628	GNDINT	GND	GND	GND
–	629	VCCINT	VCCINT	VCCINT	VCCINT
8	630	I/O	F5	E3	G6
8	631	I/O	–	–	G5
8	632	I/O	F6	E5	F6
8	633	I/O	–	–	F5
–	634	VCCIO	VCCIO8	VCCIO8	VCCIO8
–	635	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	636	I/O	–	A4	E6
1	637	I/O	–	B4	E5
1	638	I/O	–	A5	E4
–	639	GNDINT	GND	GND	GND
–	640	VCCINT	VCCINT	VCCINT	VCCINT
1	641	I/O	–	B5	D5
1	642	I/O	–	C6	C5
–	643	–	–	–	–
–	644	GNDIO	GND	GND	GND
1	645	I/O, DATA5 *(8)*	E7	F6	A5
1	646	I/O	D6	C5	F7
1	647	I/O	B3	E6	E7
1	648	I/O	C5	F7	H8
1	649	I/O	A2	A7	G8
1	650	I/O	B4	D6	F8
1	651	I/O	E8	D7	E8
1	652	I/O	D7	J11	D8
1	653	I/O	C6	B7	C8
1	654	I/O	A3	H10	B8
–	655	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	656	I/O, DATA4 *(8)*	B5	G9	B5
1	657	I/O	E9	C7	H9
1	658	I/O	A4	G10	G9

Table 63. EP20K600E I/O Pins (Part 20 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	659	I/O	D8	E7	F9
1	660	I/O	C7	F8	E9
1	661	I/O	B6	C8	D9
1	662	I/O	A5	E8	C9
1	663	I/O	D9	D8	B9
1	664	I/O	E10	H11	H10
1	665	I/O	C8	A9	G10
–	666	GNDIO	GND	GND	GND
1	667	I/O, DATA3 *(8)*	B7	F10	A8
1	668	I/O	A6	K12	F10
1	669	I/O	D10	D9	E10
1	670	I/O	C9	F9	D10
1	671	I/O	E11	E9	C10
1	672	I/O	B8	G11	B10
1	673	I/O	A7	C9	G11
1	674	I/O	D11	G12	F11
1	675	I/O	C10	B9	E11
1	676	I/O	B9	F11	G12
–	677	VCCIO	VCCIO1	VCCIO1	VCCIO1
–	678	VCCINT	VCCINT	VCCINT	VCCINT
–	679	VCCINT	VCCINT	VCCINT	VCCINT
–	680	GNDINT	GND	GND	GND
–	681	GNDINT	GND	GND	GND
1	682	I/O, DATA2 *(8)*	A8	J12	A9
1	683	I/O	C11	E10	F12
1	684	I/O	B10	H12	E12
1	685	I/O	A9	D10	G13
1	686	I/O	E13	J13	F13
1	687	I/O	D13	C10	E13
1	688	I/O	C12	B10	D13
1	689	I/O	B11	E11	C13
1	690	I/O	E14	D11	B13
1	691	I/O	A10	D12	G14
–	692	GNDIO	GND	GND	GND
1	693	I/O, DATA1 *(8)*	C13	K13	A10

Table 63. EP20K600E I/O Pins (Part 21 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	694	I/O	B12	A10	F14
1	695	I/O	D14	E12	E14
1	696	I/O	A11	A11	D14
1	697	I/O	E15	F12	C14
1	698	I/O	C14	H13	B14
1	699	I/O	B13	B12	G15
1	700	I/O	A12	B11	F15
1	701	I/O	A13	D13	E15
1	702	I/O	D15	A12	D15
–	703	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	704	I/O, CLKUSR *(8)*	C15	K14	A13
1	705	I/O	E16	D14	C15
1	706	I/O	B14	D15	B15
1	707	I/O, RDYnBSY *(8)*	A14	J14	A14
1	708	I/O	B15	C11	G16
1	709	I/O	A15	B13	F16
1	710	I/O	D16	C12	E16
1	711	I/O, INITDONE *(8)*	C16	J15	A15
1	712	I/O	B16	B14	D16
1	713	I/O	A16	C14	C16
–	714	GNDINT	GND	GND	–
–	715	TDO *(5)*	C17	G13	A18
1	716	FAST2	B17	F13	A19
–	717	GNDIO	GND	GND	GND
–	718	VCCINT	VCCINT	VCCINT	VCCINT
–	719	VCCINT	VCCINT	VCCINT	VCCINT
–	720	GNDINT	GND	GND	GND
–	721	GNDINT	GND	GND	GND
1	722	FAST1	B19	H14	A20
–	723	NCEO	C19	G14	A23
–	724	TRST *(5)*	D19	F14	A24
2	725	I/O	A20	A15	C17
2	726	I/O	B20	B15	D17
2	727	I/O	C20	C15	E17
2	728	I/O	D20	B16	F17

Table 63. EP20K600E I/O Pins (Part 22 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	729	I/O	A21	C16	G17
2	730	I/O	B21	J16	B18
2	731	I/O	A22	K15	C18
2	732	I/O	B22	G15	D18
2	733	I/O	E20	L14	E18
2	734	I/O	C21	E13	F18
–	735	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	736	I/O	D21	H15	G18
2	737	I/O	A23	E14	B19
2	738	I/O	A24	A17	C19
2	739	I/O	B23	F15	D19
2	740	I/O	C22	B17	E19
2	741	I/O	E21	D16	F19
2	742	I/O	A25	E15	G19
2	743	I/O	D22	C17	B20
2	744	I/O	B24	H16	C20
2	745	I/O	C23	A18	D20
–	746	GNDIO	GND	GND	GND
2	747	I/O	A26	G16	E20
2	748	I/O	E22	E16	F20
2	749	I/O	B25	J17	G20
2	750	I/O	C24	D17	H20
2	751	I/O	D23	F16	E21
2	752	I/O	E23	H17	F21
2	753	I/O	A27	B18	G21
2	754	I/O	B26	G17	H21
2	755	I/O	C25	C18	E22
2	756	I/O	A28	F17	F22
–	757	GNDINT	–	–	–
–	758	VCCINT	VCCINT	VCCINT	VCCINT
–	759	VCCINT	VCCINT	VCCINT	VCCINT
–	760	GNDINT	GND	GND	GND
–	761	GNDINT	GND	GND	GND
–	762	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	763	I/O	B27	D18	G22

Table 63. EP20K600E I/O Pins (Part 23 of 23)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	764	I/O	C26	E17	H22
2	765	I/O	D25	C19	B23
2	766	I/O	A29	F18	C23
2	767	I/O	B28	A20	D23
2	768	I/O	E25	B20	E23
2	769	I/O	C27	E18	F23
2	770	I/O	D26	D19	G23
2	771	I/O	A30	G18	H23
2	772	I/O	B29	C20	B24
–	773	GNDIO	GND	GND	GND
2	774	I/O	C28	H18	C24
2	775	I/O	E26	D20	D24
2	776	I/O	D27	K18	E24
2	777	I/O	A31	E19	F24
2	778	I/O	B30	F19	G24
2	779	I/O	C29	G19	H24
2	780	I/O	D28	A22	A25
2	781	I/O	A32	J19	B25
2	782	I/O	E27	E20	C25
2	783	I/O	B31	C21	D25
–	784	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	785	I/O	A33	D21	E25
2	786	I/O	C30	F20	F25
2	787	I/O	D29	B22	G25
2	788	I/O	E28	E21	H25
2	789	I/O	B32	A23	E26
2	790	I/O	A34	B23	F26
2	791	I/O	C31	F23	G26
2	792	I/O	B33	C22	E27
2	793	I/O	D30	G23	F27
2	794	I/O	E29	C23	A28
–	795	GNDIO	GND	GND	GND

Table 64 shows configuration and power pin information for EP20K600E devices in 652-pin BGA, 672-pin FineLine BGA, and 1,020-pin FineLine BGA packages.

Table 64. EP20K600E Configuration & Power Pins (Part 1 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
MSEL0 *(5)*	U35	N21	J30
MSEL1 *(5)*	W35	N20	K30
NSTATUS *(5)*	AN17	AA13	AM14
NCONFIG *(5)*	W32	P21	R30
DCLK *(5)*	U3	N7	W3
CONF_DONE *(5)*	AM17	AA12	AM13
INIT_DONE *(7)*	C16	J15	A15
nCE *(5)*	U1	P6	AC3
nCEO *(5)*	C19	G14	A23
nWS *(8)*	M1	P9	C4
nRS *(8)*	N1	N10	D4
nCS *(8)*	P2	M9	D3
CS *(8)*	R2	T6	E3
RDYnBSY *(8)*	A14	J14	A14
CLKUSR *(8)*	C15	K14	A13
DATA7 *(8)*	M6	M10	B4
DATA6 *(8)*	L6	L8	A4
DATA5 *(8)*	E7	F6	A5
DATA4 *(8)*	B5	G9	B5
DATA3 *(8)*	B7	F10	A8
DATA2 *(8)*	A8	J12	A9
DATA1 *(8)*	C13	K13	A10
DATA0 *(5)*, *(9)*	U4	N6	V3
TDI *(5)*	W1	P7	AD3
TDO *(5)*	C17	G13	A18
TCK *(5)*	AN19	AA14	AM19
TMS *(5)*	AM19	AA15	AM20
TRST *(5)*	D19	F14	A24
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14	AM18, AM15, A19, A20
CLK1p	W34	P20	N30
CLK2p	U2	N8	Y3
CLK3p	Y34	M19	W30

Table 64. EP20K600E Configuration & Power Pins (Part 2 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
CLK4p	T2	R6	P3
LOCK1 *(2)*	AA30	L21	AC30
LOCK2 *(2)*	AB6	U6	AK4
LOCK3 *(2)*	R31	L18	H30
LOCK4 *(2)*	AC6	W7	AK5
CLKLK_ENA *(5)*, *(6)*	W33	P16	P30
CLKLK_OUT1p	U31	AE23	AM29
CLKLK_OUT2p	Y3	T7	AH3
CLKLK_FB1p	Y32	AE20	AL28
CLKLK_FB2p	T4	U8	K3
DEV_CLRn *(7)*	T6	R9	H3
DEV_OE *(7)*	Y5	R8	AE3
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24	A2, B1, F1, F2, L1, L2, U1, U2, U3, AB1, AB2, AG1, AG2, AL1, AM2, AL6, AM6, AL11, AM11, AL17, AM17, AL22, AM22, AL27, AM27, AM31, AL32, AG31, AG32, AB31, AB32, T30, T31, T32, L31, L32, F31, F32, B32, A31, A27, B27, A22, B22, A16, B16, A11, B11, A6, B6
VCCIO1	C4, D5, E17	A6, J10, L12	A12, B12, A7, B7, A3
VCCIO2	E19, D31, C32	A13, K16,M14, A16	A30, A26, B26, A21, B21
VCCIO3	F30, F31, U30	A21, L17, N15	M31, M32, G31, G32, C32
VCCIO4	W30, AL31, AL32	N24, R16, U18	AK32, AF31, AF32, AA31, AA32
VCCIO5	AN32, AN33, AL19	T15, V17, AF21	AL21, AM21, AL26, AM26, AM30
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13	AM3, AL7, AM7, AL12, AM12
VCCIO7	AL3, AL4, W6	P12, T10, AF6	AA1, AA2, AF1, AF2, AK1
VCCIO8	U6, E3, E4	K9, M11, N3	C1, G1, G2, M1, M2
VCC_CKLK1 *(10)*	AA35	AF18	W24
VCC_CKLK2 *(10)*	W4	N11	Y9
VCC_CKLK3 *(10)*	T34	AC26	M24
VCC_CKLK4 *(10)*	R4	P10	P9
VCC_CKOUT1 *(4)*	U33	AF22	N24
VCC_CKOUT2 *(4)*	Y1	V7	AA9

Table 64. EP20K600E Configuration & Power Pins (Part 3 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D18, D2, D3, D17, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26 R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, AF15	B2, B3, C2, C3, F3, F4, G3, G4, L3, L4, M3, M4, T1, T2, T3, AA3, AA4, AB3, AB4, AF3, AF4, AG3, AG4, AK2, AK3, AL2, AL3, AJ6, AJ7, AK6, AK7, AJ11, AJ12, AK11, AK12, AL16, AM16, AJ21, AJ22, AK21, AK22, AJ26, AJ27, AK26, AK27, AK30, AK31, AL30, AL31, AG29, AG30, AF29, AF30, AB29, AB30, AA29, AA30, U30, U31, U32, M29, M30, L29, L30, G29, G30, F29, F30, C30, C31, B30, B31, C26, C27, D26, D27, C21, C22, D21, D22, A17, B17, C11, C12, D11, D12, C6, C7, D6, D7
GND_CKLK1 *(10)*	Y30	AE18	V24
GND_CKLK2 *(10)*	W2	P11	V9
GND_CKLK3 *(10)*	T33, V35	AC25, N25	P24, P23
GND_CKLK4 *(3)*	R3	R10	T9
GND_CKOUT1 *(4)*	U32	AE22	T24
GND_CKOUT2 *(4)*	Y2	V6	W9

Table 64. EP20K600E Configuration & Power Pins (Part 4 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
No Connect (N.C.)			AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB8, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AC24, AC25, AC8, AC9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AD24, AD25, AD8, AD9, AE14,AE15, AE16, AE17, AE18, AE19, H11, H12, H13, H14, H15, H16, H17, H18, H19, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K20, K21, K22, K23, K24, K25, K9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L9, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, N12, N13, N14, N15, N16, N17, N18, N19, N20, N21, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21
Total User I/O Pins *(11)*	488	508	588

Notes to tables:

(1) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for LVDS standard. If not used for the LVDS pair, these pins are regular I/Os. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.
(2) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(3) The CLKLK_OUT and CLKLK_FBIN pins are powered by the VCC_CKOUT and GND_CKOUT pins.
(4) This pin is the power or ground for the external output and feedback input of a PLL. These pins should be set to the V_{CCIO} level/standard desired for the external clock output and feedback input (if used). To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the V_{CCIO} and GND_{IO} pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GND_{IO}, respectively.
(5) This pin is a dedicated pin; it is not available as a user I/O pin.
(6) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will begin lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.
(7) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(8) This pin can be used as a user I/O pin after configuration.
(9) This pin is tri-stated in user mode.
(10) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Table 65 shows I/O pin information for EP20K1000E devices in 652-pin BGA, 672-pin FineLine BGA, and 1,020-pin FineLine BGA packages.

Table 65. EP20K1000E I/O Pins (Part 1 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	1	I/O	–	H23	B28
2	2	I/O	–	E24	C29
–	3	VCCINT	VCCINT	VCCINT	VCCINT
–	4	GNDINT	GND	GND	GND
2	5	I/O	–	F24	C28
2	6	I/O	–	D22	D30
2	7	I/O	–	E23	D29
–	8	VCCIO	VCCIO2	VCCIO2	VCCIO2
–	9	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	10	I/O	–	–	D28
3	11	I/O	F32	E22	E30
3	12	I/O	–	–	E29
3	13	I/O	F33	F21	E28

Table 65. EP20K1000E I/O Pins (Part 2 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	14	VCCINT	VCCINT	VCCINT	VCCINT
–	15	GNDINT	GND	GND	GND
3	16	I/O	–	–	F28
3	17	I/O	–	–	G28
3	18	I/O	E34	G20	G27
3	19	I/O	–	–	H29
3	20	I/O	D35	F22	H28
–	21	GNDIO	GND	GND	GND
3	22	I/O	–	–	H27
3	23	I/O	–	–	H26
3	24	I/O	G31	J21	J29
3	25	I/O	–	–	J28
3	26	I/O	G32	G21	J27
–	27	VCCINT	VCCINT	VCCINT	VCCINT
–	28	GNDINT	GND	GND	GND
3	29	I/O	–	–	J26
3	30	I/O	–	–	K29
3	31	I/O	G33	H21	K28
3	32	I/O	–	–	K27
3	33	I/O	F34	G24	K26
–	34	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	35	I/O	–	–	L28
3	36	I/O	–	–	L27
3	37	I/O	E35	J22	L26
3	38	I/O	–	–	M28
3	39	I/O	G34	H22	M27
–	40	VCCINT	VCCINT	VCCINT	VCCINT
–	41	GNDINT	GND	GND	GND
3	42	I/O	–	–	M26
3	43	I/O	–	–	M25
3	44	I/O	H30	H20	M23
3	45	I/O	–	–	M22
3	46	I/O	H31	G22	N29
–	47	GNDIO	GND	GND	GND
3	48	I/O	–	–	N28

Table 65. EP20K1000E I/O Pins (Part 3 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	49	I/O	–	–	N27
3	50	I/O	H32	J20	N26
3	51	I/O	–	–	N25
3	52	I/O	H33	K19	N23
–	53	VCCINT	VCCINT	VCCINT	VCCINT
–	54	GNDINT	GND	GND	GND
–	55	VCCINT	VCCINT	VCCINT	VCCINT
–	56	GNDINT	GND	GND	GND
3	57	I/O, LVDSRX16p	H34	D26	D31
3	58	I/O, LVDSRX16n *(1)*	G35	D25	D32
3	59	I/O	J30	H24	N22
3	60	I/O, LVDSRX15n *(1)*	J31	E26	E31
3	61	I/O, LVDSRX15p	J32	E25	E32
–	62	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	63	I/O, LVDSRX14p	J33	F26	H31
3	64	I/O, LVDSRX14n *(1)*	J34	F25	H32
3	65	I/O	H35	K24	P29
3	66	I/O, LVDSRX13n *(1)*	J35	G26	J31
3	67	I/O, LVDSRX13p	K30	G25	J32
–	68	VCCINT	VCCINT	VCCINT	VCCINT
–	69	GNDINT	GND	GND	GND
3	70	I/O, LVDSRX12p	K32	H26	K31
3	71	I/O, LVDSRX12n *(1)*	K33	H25	K32
3	72	I/O	K34	K22	P28
3	73	I/O, LVDSRX11n *(1)*	K35	J26	N31
3	74	I/O, LVDSRX11p	L30	J25	N32
–	75	GNDIO	GND	GND	GND
3	76	I/O, LVDSRX10p	L31	K26	P31
3	77	I/O, LVDSRX10n *(1)*	L32	K25	P32
3	78	I/O	L33	K20	P27
3	79	I/O, LVDSRX09n *(1)*	L34	L26	R31
3	80	I/O, LVDSRX09p	L35	L25	R32
–	81	VCCINT	VCCINT	VCCINT	VCCINT
–	82	GNDINT	GND	GND	GND
3	83	I/O, LVDSRX08p	M31	M26	V31

Table 65. EP20K1000E I/O Pins (Part 4 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	84	I/O, LVDSRX08n *(1)*	M32	M25	V32
3	85	I/O	M33	K23	P26
3	86	I/O, LVDSRX07n *(1)*	M34	R26	W31
3	87	I/O, LVDSRX07p	M35	R25	W32
–	88	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	89	I/O, LVDSRX06p	N30	T26	Y31
3	90	I/O, LVDSRX06n *(1)*	N31	T25	Y32
3	91	I/O	N32	K21	P25
3	92	I/O, LVDSRX05n *(1)*	N33	U26	AC31
3	93	I/O, LVDSRX05p	N34	U25	AC32
–	94	VCCINT	VCCINT	VCCINT	VCCINT
–	95	GNDINT	GND	GND	GND
3	96	I/O, LVDSRX04p	P30	V26	AD31
3	97	I/O, LVDSRX04n *(1)*	P31	V25	AD32
3	98	I/O	P32	J24	P22
3	99	I/O, LVDSRX03n *(1)*	P33	W26	AE31
3	100	I/O, LVDSRX03p	P34	W25	AE32
–	101	GNDIO	GND	GND	GND
3	102	I/O, LVDSRX02p	P35	Y26	AH31
3	103	I/O, LVDSRX02n *(1)*	R30	Y25	AH32
3	104	I/O, LOCK3 *(2)*	R31	L18	H30
3	105	I/O, LVDSRX01n *(1)*	R32	AA26	AJ31
3	106	I/O, LVDSRX01p	R33	AA25	AJ32
–	107	VCCINT	VCCINT	VCCINT	VCCINT
–	108	GNDINT	GND	GND	GND
3	109	I/O	R35	L19	R29
3	110	I/O	T30	J23	R28
3	111	I/O, LVDSRXINCLK1n *(1)*	T31	AB26	A29
3	112	I/O, LVDSRXINCLK1p	T32	AB25	B29
–	113	GND_CKLK3 *(3)*	T33	AC25	P24
–	114	GND_CKLK3 *(3)*	V35	N25	P23
–	115	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	116	VCC_CKLK3 *(3)*	T34	AC26	M24
3	117	I/O, CLKLK_OUT1n *(1)*	T35	AF23	AL29
–	118	CLKLK_OUT1p *(4)*	U31	AE23	AM29

Table 65. EP20K1000E I/O Pins (Part 5 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	119	GND_CKOUT1 *(5)*	U32	AE22	T24
–	120	VCC_CKOUT1 *(5)*	U33	AF22	N24
–	121	VCCINT	VCCINT	VCCINT	VCCINT
–	122	GNDINT	GND	GND	GND
–	123	MSEL0 *(6)*	U35	N21	J30
–	124	MSEL1 *(6)*	W35	N20	K30
4	125	CLK1p	W34	P20	N30
–	126	CLKLK_ENA *(6)*, *(7)*	W33	P16	P30
–	127	nCONFIG *(6)*	W32	P21	R30
–	128	GNDINT	GND	GND	GND
–	129	VCCINT	VCCINT	VCCINT	VCCINT
4	130	I/O, CLK1n *(1)*	Y35	P19	V30
4	131	CLK3p	Y34	M19	W30
4	132	I/O, CLK3n *(1)*	Y33	M20	Y30
4	133	CLKLK_FB1p *(4)*	Y32	AE20	AL28
4	134	I/O, CLKLK_FB1n *(1)*	Y31	AF20	AM28
–	135	GNDIO	GND	GND	GND
–	136	GND_CKLK1 *(3)*	Y30	AE18	V24
–	137	GND_CKLK1 *(3)*	Y30	AE18	V24
–	138	VCC_CKLK1 *(3)*	AA35	AF18	W24
4	139	I/O	AA34	N23	R27
4	140	I/O	AA33	L24	R26
4	141	I/O	AA32	L23	R25
–	142	GNDINT	GND	GND	GND
–	143	VCCINT	VCCINT	VCCINT	VCCINT
4	144	I/O, LOCK1 *(2)*	AA30	L21	AC30
4	145	I/O	AB35	L22	R24
4	146	I/O	AB34	M23	R23
4	147	I/O	AB33	R22	R22
4	148	I/O	AB32	M22	T29
–	149	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	150	I/O	AB31	M24	T28
4	151	I/O	AB30	M21	T27
4	152	I/O	AC35	T24	T26
4	153	I/O	AC34	R24	T25

Table 65. EP20K1000E I/O Pins (Part 6 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	154	I/O	AC33	U24	T23
–	155	GNDINT	GND	GND	GND
–	156	VCCINT	VCCINT	VCCINT	VCCINT
4	157	I/O	AC31	R23	T22
4	158	I/O	AC30	T23	U29
4	159	I/O	AD35	M18	U28
4	160	I/O	AD34	T22	U27
4	161	I/O	AD33	M17	U26
–	162	GNDIO	GND	GND	GND
4	163	I/O	AD32	L20	U25
4	164	I/O	AD31	N22	U24
4	165	I/O	AD30	N19	U23
4	166	I/O	AE35	U23	U22
4	167	I/O	AE34	N18	V29
–	168	GNDINT	GND	GND	GND
–	169	VCCINT	VCCINT	VCCINT	VCCINT
4	170	I/O	AE32	P22	V28
4	171	I/O	AE31	R20	V27
4	172	I/O	AE30	U22	V26
4	173	I/O	AF35	R21	V25
4	174	I/O	AF34	T21	V23
–	175	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	176	I/O	AF33	N17	V22
4	177	I/O	AF32	P18	W29
4	178	I/O	AF31	V23	W28
4	179	I/O	AF30	R19	W27
4	180	I/O	AG35	V22	W26
–	181	GNDINT	GND	GND	GND
–	182	VCCINT	VCCINT	VCCINT	VCCINT
4	183	I/O	AG34	N16	W25
4	184	I/O	AG33	V24	W23
4	185	I/O	AG32	T20	W22
4	186	I/O	AG31	W24	Y29
4	187	I/O	AG30	R18	Y28
–	188	GNDIO	GND	GND	GND

Table 65. EP20K1000E I/O Pins (Part 7 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	189	I/O	AJ35	P17	Y27
4	190	I/O	AH34	U21	Y26
4	191	I/O	AK35	T19	Y25
4	192	I/O	AH33	W23	Y24
4	193	I/O	AH32	R17	Y23
–	194	GNDINT	GND	GND	GND
–	195	VCCINT	VCCINT	VCCINT	VCCINT
–	196	GNDINT	GND	GND	GND
–	197	VCCINT	VCCINT	VCCINT	VCCINT
4	198	I/O	AH30	U20	Y22
4	199	I/O	–	–	AA28
4	200	I/O	AJ34	AA22	AA27
4	201	I/O	–	–	AA26
4	202	I/O	–	–	AA25
–	203	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	204	I/O	AL35	W22	AA24
4	205	I/O	–	–	AA23
4	206	I/O	AK34	Y21	AA22
4	207	I/O	–	–	AB28
4	208	I/O	–	–	AB27
–	209	GNDINT	GND	GND	GND
–	210	VCCINT	VCCINT	VCCINT	VCCINT
4	211	I/O	AJ33	V21	AB26
4	212	I/O	–	–	AC29
4	213	I/O	AJ32	V20	AC28
4	214	I/O	–	–	AC27
4	215	I/O	–	–	AC26
–	216	GNDIO	GND	GND	GND
4	217	I/O	AJ31	W21	AD30
4	218	I/O	–	–	AD29
4	219	I/O	AJ30	T18	AD28
4	220	I/O	–	–	AD27
4	221	I/O	–	–	AD26
–	222	GNDINT	GND	GND	GND
–	223	VCCINT	VCCINT	VCCINT	VCCINT

Table 65. EP20K1000E I/O Pins (Part 8 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	224	I/O	AM35	V19	AE30
4	225	I/O	–	–	AE29
4	226	I/O	AL34	AB22	AE28
4	227	I/O	–	–	AE27
4	228	I/O	–	–	AE26
–	229	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	230	I/O	AK32	U19	AF28
4	231	I/O	–	–	AF27
4	232	I/O	AK31	AB21	AG28
4	233	I/O	–	–	AG27
4	234	I/O	–	–	AH30
–	235	GNDINT	GND	GND	GND
–	236	VCCINT	VCCINT	VCCINT	VCCINT
4	237	I/O	AK30	Y22	AH29
4	238	I/O	–	–	AH28
4	239	I/O	AL33	AA21	AJ30
4	240	I/O	–	–	AJ29
–	241	GNDIO	GND	GND	GND
5	242	I/O	–	AB23	AJ28
5	243	I/O	–	AA24	AK29
5	244	I/O	–	AA23	AK28
–	245	GNDINT	GND	GND	GND
–	246	VCCINT	VCCINT	VCCINT	VCCINT
5	247	I/O	–	Y24	AH27
5	248	I/O	–	Y23	AF26
5	249	I/O	AL29	AC21	AG26
5	250	I/O	–	–	AH26
5	251	I/O	AM30	AC22	AB25
5	252	I/O	–	–	AC25
5	253	I/O	AP33	AB24	AD25
–	254	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	255	I/O	AN31	AA20	AE25
5	256	I/O	AR34	AD23	AF25
5	257	I/O	AP32	AC20	AG25
5	258	I/O	AL28	AB19	AH25

Table 65. EP20K1000E I/O Pins (Part 9 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	259	I/O	AM29	AB20	AJ25
5	260	I/O	–	–	AK25
5	261	I/O	AN30	Y20	AL25
5	262	I/O	–	–	AM25
5	263	I/O	AR33	AC19	AB24
5	264	I/O	–	–	AC24
–	265	GNDIO	GND	GND	GND
5	266	I/O	–	–	AD24
5	267	I/O	AP31	W20	AE24
5	268	I/O	–	–	AF24
5	269	I/O	AL27	AD22	AG24
5	270	I/O	–	–	AH24
5	271	I/O	AR32	Y19	AJ24
5	272	I/O	AM28	AD21	AK24
5	273	I/O	AN29	AA19	AL24
5	274	I/O	AP30	W18	AM24
5	275	I/O	AR31	AF17	AB23
–	276	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	277	I/O	AM27	Y18	AC23
5	278	I/O	–	–	AD23
5	279	I/O	AL26	AE17	AE23
5	280	I/O	–	–	AF23
5	281	I/O	AN28	W17	AG23
5	282	I/O	–	–	AH23
5	283	I/O	–	–	AJ23
5	284	I/O	AP29	AC18	AK23
5	285	I/O	–	–	AL23
5	286	I/O	AR30	AA18	AM23
–	287	GNDIO	GND	GND	GND
5	288	I/O	–	–	AB22
5	289	I/O	AM26	AF16	AC22
5	290	I/O	AN27	Y17	AD22
5	291	I/O	AL25	AB18	AE22
5	292	I/O	AP28	AD20	AF22
5	293	I/O	AR29	AA17	AG22

Table 65. EP20K1000E I/O Pins (Part 10 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	294	I/O	AM25	AE16	AH22
5	295	I/O	–	–	AB21
5	296	I/O	AN26	V16	AC21
5	297	I/O	–	–	–
5	298	I/O	AP27	AB17	AD21
–	299	GNDINT	GND	GND	GND
–	300	GNDINT	GND	GND	GND
–	301	VCCINT	VCCINT	VCCINT	VCCINT
–	302	VCCINT	VCCINT	VCCINT	VCCINT
–	303	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	304	I/O	AR28	U15	AE21
5	305	I/O	–	–	–
5	306	I/O	AN25	AC17	AF21
5	307	I/O	–	–	AG21
5	308	I/O	AP26	W16	AH21
5	309	I/O	AR27	AC16	AB20
5	310	I/O	AL23	Y16	AC20
5	311	I/O	AM23	AA16	AD20
5	312	I/O	AN24	AD19	AE20
5	313	I/O	AP25	T14	AF20
5	314	I/O	–	–	AG20
–	315	GNDIO	GND	GND	GND
5	316	I/O	AL22	AB16	AH20
5	317	I/O	–	–	AJ20
5	318	I/O	AR26	W15	AK20
5	319	I/O	–	–	AL20
5	320	I/O	–	–	AB19
5	321	I/O	AN23	AB15	AC19
5	322	I/O	–	–	AD19
5	323	I/O	AP24	V15	AE19
5	324	I/O	–	–	AF19
5	325	I/O	AM22	AC15	AG19
–	326	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	327	I/O	AR25	U14	AH19
5	328	I/O	AL21	AD18	AJ19

Table 65. EP20K1000E I/O Pins (Part 11 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	329	I/O	AN22	AC11	AK19
5	330	I/O	AP23	Y15	AL19
5	331	I/O	AR24	AB14	AB18
5	332	I/O	–	–	AC18
5	333	I/O	AR23	V14	AD18
5	334	I/O	–	–	AE18
5	335	I/O	AM21	AB13	AF18
5	336	I/O	–	–	AG18
–	337	GNDIO	GND	GND	GND
5	338	I/O	–	–	AH18
5	339	I/O	AN21	AD10	AJ18
5	340	I/O	–	–	AK18
5	341	I/O	AL20	AC14	AL18
5	342	I/O	–	–	AB17
5	343	I/O	AP22	AC12	AC17
5	344	I/O	AR22	AD17	AD17
5	345	I/O	AP21	AC13	AE17
5	346	I/O	AR21	AD16	AF17
5	347	I/O	AM20	AD15	AG17
–	348	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	349	I/O	AN20	AE15	AH17
5	350	I/O	–	–	AJ17
5	351	I/O	AP20	AD14	AK17
5	352	I/O	–	–	AK16
5	353	I/O	AR20	AE14	AJ16
–	354	TMS *(6)*	AM19	AA15	AM20
–	355	TCK *(6)*	AN19	AA14	AM19
5	356	FAST3	AP19	Y14	AM18
–	357	GNDIO	GND	GND	GND
–	358	GNDINT	GND	GND	GND
–	359	GNDINT	GND	GND	GND
–	360	VCCINT	VCCINT	VCCINT	VCCINT
–	361	VCCINT	VCCINT	VCCINT	VCCINT
5	362	FAST4	AP17	Y13	AM15
–	363	NSTATUS *(6)*	AN17	AA13	AM14

Table 65. EP20K1000E I/O Pins (Part 12 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	364	CONF_DONE *(6)*	AM17	AA12	AM13
6	365	I/O	AR16	AE13	AH16
6	366	I/O	–	–	AG16
6	367	I/O	AP16	AF12	AF16
6	368	I/O	–	–	AE16
6	369	I/O	AN16	AE12	AD16
–	370	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	371	I/O, LVDSDESKEW	AM16	U12	AM10
6	372	I/O	AR15	AD12	AC16
6	373	I/O	AP15	AD11	AB16
6	374	I/O	AR14	V13	AL15
6	375	I/O	AP14	AE11	AK15
6	376	I/O	–	–	AJ15
6	377	I/O	AL16	W13	AH15
6	378	I/O	–	–	AG15
6	379	I/O	AN15	U13	AF15
6	380	I/O	–	–	AE15
–	381	GNDIO	GND	GND	GND
6	382	I/O	–	–	AD15
6	383	I/O	AM15	AF10	AC15
6	384	I/O	–	–	AB15
6	385	I/O	AR13	AB12	AL14
6	386	I/O	–	–	AK14
6	387	I/O	AR12	W14	AJ14
6	388	I/O	AP13	T13	AH14
6	389	I/O	AN14	Y12	AG14
6	390	I/O	AL15	W12	AF14
6	391	I/O	AR11	AE10	AE14
–	392	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	393	I/O	AM14	V12	AD14
6	394	I/O	–	–	AC14
6	395	I/O	AP12	AF11	AB14
6	396	I/O	–	–	AL13
6	397	I/O	AN13	W11	AK13
6	398	I/O	–	–	AJ13

Table 65. EP20K1000E I/O Pins (Part 13 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
6	399	I/O	–	–	AH13
6	400	I/O	AR10	AF9	AG13
6	401	I/O	–	–	AF13
6	402	I/O	AL14	Y11	AE13
–	403	GNDIO	GND	GND	GND
6	404	I/O	–	–	AD13
6	405	I/O	AP11	AE9	AC13
6	406	I/O	AN12	AA11	AB13
6	407	I/O	AM13	AC10	AH12
6	408	I/O	AL13	AB10	AG12
6	409	I/O	AR9	V11	AF12
6	410	I/O	AP10	AB11	AE12
6	411	I/O	–	–	AD12
6	412	I/O	AN11	AA10	AC12
6	413	I/O	–	–	–
6	414	I/O	AR8	AD9	AB12
–	415	GNDINT	GND	GND	GND
–	416	GNDINT	GND	GND	GND
–	417	VCCINT	VCCINT	VCCINT	VCCINT
–	418	VCCINT	VCCINT	VCCINT	VCCINT
–	419	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	420	I/O	AP9	Y10	AH11
6	421	I/O	–	–	–
6	422	I/O	AN10	AC9	AG11
6	423	I/O	–	–	AF11
6	424	I/O	AM11	W10	AE11
6	425	I/O	AR7	AB9	AD11
6	426	I/O	AP8	W9	AC11
6	427	I/O	AL11	Y9	AB11
6	428	I/O	AN9	AD8	AL10
6	429	I/O	AM10	Y8	AK10
6	430	I/O	–	–	AJ10
–	431	GNDIO	GND	GND	GND
6	432	I/O	AR6	AC8	AH10
6	433	I/O	–	–	AG10

Table 65. EP20K1000E I/O Pins (Part 14 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
6	434	I/O	AP7	AA8	AF10
6	435	I/O	–	–	AE10
6	436	I/O	–	–	AD10
6	437	I/O	AN8	AF7	AC10
6	438	I/O	–	–	AB10
6	439	I/O	AL10	AA9	AM9
6	440	I/O	–	–	AL9
6	441	I/O	AM9	AE7	AK9
–	442	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	443	I/O	AR5	T9	AJ9
6	444	I/O	AP6	AD7	AH9
6	445	I/O	AN7	AC7	AG9
6	446	I/O	AM8	V8	AF9
6	447	I/O	AR4	AF5	AE9
6	448	I/O	–	–	AD9
6	449	I/O	AL9	AB8	AC9
6	450	I/O	–	–	AB9
6	451	I/O	AP5	AC6	AM8
6	452	I/O	–	–	AL8
–	453	GNDIO	GND	GND	GND
6	454	I/O	–	–	AK8
6	455	I/O	AR3	Y7	AJ8
6	456	I/O	–	–	AH8
6	457	I/O	AN6	AB7	AG8
6	458	I/O	–	–	AF8
6	459	I/O	AM7	AD6	AE8
6	460	I/O	AL8	AD5	AD8
6	461	I/O	AP4	AE5	AC8
6	462	I/O	AR2	AA3	AB8
6	463	I/O	AN5	AD4	AH7
–	464	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	465	I/O	AP3	Y3	AG7
6	466	I/O	–	–	AF7
6	467	I/O	AM6	AF4	AH6
6	468	I/O	–	–	AJ5

Table 65. EP20K1000E I/O Pins (Part 15 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
6	469	I/O	AL7	AB3	AJ4
6	470	I/O	–	AE4	AH5
6	471	I/O	–	Y4	AH4
–	472	VCCINT	VCCINT	VCCINT	VCCINT
–	473	GNDINT	GND	GND	GND
6	474	I/O	–	AC5	AG6
6	475	I/O	–	AA4	AG5
6	476	I/O	–	AB4	AF6
–	477	GNDIO	GND	GND	GND
7	478	I/O	–	–	AF5
7	479	I/O	AK6	AB6	AE7
7	480	I/O	–	–	AE6
7	481	I/O	AK5	AA7	AE5
–	482	VCCINT	VCCINT	VCCINT	VCCINT
–	483	GNDINT	GND	GND	GND
7	484	I/O	–	–	AE4
7	485	I/O	–	–	AD7
7	486	I/O	AK4	AA6	AD6
7	487	I/O	–	–	AD5
7	488	I/O	AK3	Y6	AD4
–	489	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	490	I/O	–	–	AC7
7	491	I/O	–	–	AC6
7	492	I/O	AM1	AA5	AC5
7	493	I/O	–	–	AC4
7	494	I/O	AJ6	AB5	AB7
–	495	VCCINT	VCCINT	VCCINT	VCCINT
–	496	GNDINT	GND	GND	GND
7	497	I/O	–	–	AB6
7	498	I/O	–	–	AB5
7	499	I/O	AJ5	Y5	AA11
7	500	I/O	–	–	AA10
7	501	I/O	AJ4	W3	AA8
–	502	GNDIO	GND	GND	GND
7	503	I/O	–	–	AA7

Table 65. EP20K1000E I/O Pins (Part 16 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	504	I/O	–	–	AA6
7	505	I/O	AJ3	V4	AA5
7	506	I/O	–	–	Y11
7	507	I/O	AK2	V5	Y10
–	508	VCCINT	VCCINT	VCCINT	VCCINT
–	509	GNDINT	GND	GND	GND
7	510	I/O	–	–	Y8
7	511	I/O	–	–	Y7
7	512	I/O	AL1	W6	Y6
7	513	I/O	–	–	Y5
7	514	I/O	AJ2	W5	Y4
–	515	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	516	I/O	–	–	W11
7	517	I/O	–	–	W10
7	518	I/O	AH6	V3	W8
7	519	I/O	–	–	W7
7	520	I/O	AH5	U3	W6
–	521	VCCINT	VCCINT	VCCINT	VCCINT
–	522	GNDINT	GND	GND	GND
–	523	VCCINT	VCCINT	VCCINT	VCCINT
–	524	GNDINT	GND	GND	GND
7	525	I/O, LVDSTX16p	AH3	AC2	AJ2
7	526	I/O, LVDSTX16n *(1)*	AK1	AC1	AJ1
7	527	I/O	AH2	W4	W5
7	528	I/O, LVDSTX15n *(1)*	AJ1	AB2	AH2
7	529	I/O, LVDSTX15p	AG6	AB1	AH1
–	530	GNDIO	GND	GND	GND
7	531	I/O, LVDSTX14p	AG5	AA2	AE2
7	532	I/O, LVDSTX14n *(1)*	AG4	AA1	AE1
7	533	I/O	AG3	U4	W4
7	534	I/O, LVDSTX13n *(1)*	AG2	Y2	AD2
7	535	I/O, LVDSTX13p	AH1	Y1	AD1
–	536	VCCINT	VCCINT	VCCINT	VCCINT
–	537	GNDINT	GND	GND	GND
7	538	I/O, LVDSTX12p	AF6	W2	AC2

Table 65. EP20K1000E I/O Pins (Part 17 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	539	I/O, LVDSTX12n *(1)*	AF5	W1	AC1
7	540	I/O	AF4	T4	V11
7	541	I/O, LVDSTX11n *(1)*	AF3	V2	Y2
7	542	I/O, LVDSTX11p	AF2	V1	Y1
–	543	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	544	I/O, LVDSTX10p	AF1	U2	W2
7	545	I/O, LVDSTX10n *(1)*	AE6	U1	W1
7	546	I/O	AE5	U5	V10
7	547	I/O, LVDSTX09n *(1)*	AE4	T2	V2
7	548	I/O, LVDSTX09p	AE3	T1	V1
–	549	VCCINT	VCCINT	VCCINT	VCCINT
–	550	GNDINT	GND	GND	GND
7	551	I/O, LVDSTX08p	AE1	R2	R2
7	552	I/O, LVDSTX08n *(1)*	AD6	R1	R1
7	553	I/O	AD5	T3	V8
7	554	I/O, LVDSTX07n *(1)*	AD4	M2	P2
7	555	I/O, LVDSTX07p	AD3	M1	P1
–	556	GNDIO	GND	GND	GND
7	557	I/O, LVDSTX06p	AD2	L2	N2
7	558	I/O, LVDSTX06n *(1)*	AD1	L1	N1
7	559	I/O, LOCK4 *(2)*	AC6	W7	AK5
7	560	I/O, LVDSTX05n *(1)*	AC5	K2	K2
7	561	I/O, LVDSTX05p	AC4	K1	K1
–	562	VCCINT	VCCINT	VCCINT	VCCINT
–	563	GNDINT	GND	GND	GND
7	564	I/O, LVDSTX04p	AC2	J2	J2
7	565	I/O, LVDSTX04n *(1)*	AC1	J1	J1
7	566	I/O	AB1	T5	V7
7	567	I/O, LVDSTX03n *(1)*	AB5	H2	H2
7	568	I/O, LVDSTX03p	AB4	H1	H1
–	569	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	570	I/O, LVDSTX02p	AB3	G2	E2
7	571	I/O, LVDSTX02n *(1)*	AB2	G1	E1
7	572	I/O	AA1	R5	V6
7	573	I/O, LVDSTX01n *(1)*	AA6	F2	D2

Table 65. EP20K1000E I/O Pins (Part 18 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	574	I/O, LVDSTX01p	AA5	F1	D1
–	575	VCCINT	VCCINT	VCCINT	VCCINT
–	576	GNDINT	GND	GND	GND
7	577	I/O, CLKLVDS_OUTp	AA3	E2	AL4
7	578	I/O, CLKLVDS_OUTn *(1)*	AA2	E1	AM4
7	579	I/O, LOCK2 *(2)*	AB6	U6	AK4
7	580	I/O, LVDSTXINCLK1n *(1)*	Y6	D2	AL5
7	581	I/O, LVDSTXINCLK1p	W5	D1	AM5
–	582	GNDIO	GND	GND	GND
7	583	I/O, CLKLK_OUT2n *(1)*	Y4	U7	AJ3
–	584	CLKLK_OUT2p	Y3	T7	AH3
–	585	GND_CKOUT2 *(5)*	Y2	V6	W9
–	586	VCC_CKOUT2 *(5)*	Y1	V7	AA9
7	587	I/O, DEV_OE *(8)*	Y5	R8	AE3
–	588	VCC_CKLK2 *(3)*	W4	N11	Y9
–	589	VCCINT	VCCINT	VCCINT	VCCINT
–	590	GNDINT	GND	GND	GND
–	591	GND_CKLK2 *(3)*	W2	P11	V9
–	592	GND_CKLK2 *(3)*	W2	P11	V9
–	593	TDI *(6)*	W1	P7	AD3
–	594	NCE *(6)*	U1	P6	AC3
–	595	CLK2p	U2	N8	Y3
–	596	DCLK *(6)*	U3	N7	W3
–	597	DATA0 *(6)*	U4	N6	V3
–	598	GNDINT	GND	GND	GND
–	599	VCCINT	VCCINT	VCCINT	VCCINT
8	600	I/O, CLK2n *(1)*	T1	N9	R3
–	601	CLK4p	T2	R6	P3
8	602	I/O, CLK4n *(1)*	T3	R7	N3
–	603	CLKLK_FB2p *(4)*	T4	U8	K3
8	604	I/O, CLKLK_FB2n *(1)*	T5	T8	J3
–	605	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	606	I/O, DEV_CLRn *(8)*	T6	R9	H3
8	607	I/O	R1	M4	V5
8	608	I/O, CS *(9)*	R2	T6	E3

Table 65. EP20K1000E I/O Pins (Part 19 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	609	GND_CKLK4 *(3)*	R3	R10	T9
–	610	GND_CKLK4 *(3)*	R3	R10	T9
–	611	VCC_CKLK4 *(3)*	R4	P10	P9
–	612	GNDINT	GND	GND	GND
–	613	VCCINT	VCCINT	VCCINT	VCCINT
8	614	I/O	R6	P5	V4
8	615	I/O	P1	R3	U11
8	616	I/O, nCS *(9)*	P2	M9	D3
8	617	I/O	P3	P4	U10
8	618	I/O	P4	M3	U9
–	619	GNDIO	GND	GND	GND
8	620	I/O	P5	M5	U8
8	621	I/O	P6	R4	U7
8	622	I/O, nRS *(9)*	N1	N10	D4
8	623	I/O	N2	L3	U6
8	624	I/O	N3	L4	U5
–	625	GNDINT	GND	GND	GND
–	626	VCCINT	VCCINT	VCCINT	VCCINT
8	627	I/O	N5	P8	U4
8	628	I/O	N6	L5	T11
8	629	I/O, nWS *(9)*	M1	P9	C4
8	630	I/O	M2	M7	T10
8	631	I/O	M3	L9	T8
–	632	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	633	I/O	M4	L7	T7
8	634	I/O	M5	M6	T6
8	635	I/O, DATA7 *(9)*	M6	M10	B4
8	636	I/O	L1	M8	T5
8	637	I/O	L2	N5	T4
–	638	GNDINT	GND	GND	GND
–	639	VCCINT	VCCINT	VCCINT	VCCINT
8	640	I/O	L4	K4	R11
8	641	I/O	L5	K6	R9
8	642	I/O, DATA6 *(9)*	L6	L8	A4
8	643	I/O	K1	K8	R10

Table 65. EP20K1000E I/O Pins (Part 20 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	644	I/O	K2	J3	R8
–	645	GNDIO	GND	GND	GND
8	646	I/O	K3	J7	R7
8	647	I/O	K4	L6	R6
8	648	I/O	K5	J6	R5
8	649	I/O	K6	K5	R4
8	650	I/O	J1	J4	P11
–	651	GNDINT	GND	GND	GND
–	652	VCCINT	VCCINT	VCCINT	VCCINT
8	653	I/O	J2	K3	P10
8	654	I/O	J3	H3	P8
8	655	I/O	J4	J8	P7
8	656	I/O	J5	H9	P6
8	657	I/O	J6	J5	P5
–	658	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	659	I/O	G1	K7	P4
8	660	I/O	H2	H6	N11
8	661	I/O	F1	H4	N10
8	662	I/O	H3	H7	N9
8	663	I/O	H4	G7	N8
–	664	GNDINT	GND	GND	GND
–	665	VCCINT	VCCINT	VCCINT	VCCINT
–	666	GNDINT	GND	GND	GND
–	667	VCCINT	VCCINT	VCCINT	VCCINT
8	668	I/O	H6	H5	N7
8	669	I/O	–	–	N6
8	670	I/O	G2	G6	N5
8	671	I/O	–	–	N4
8	672	I/O	–	–	M11
–	673	GNDIO	GND	GND	GND
8	674	I/O	E1	C4	M10
8	675	I/O	–	–	M9
8	676	I/O	F2	G4	M8
8	677	I/O	–	–	M7
8	678	I/O	–	–	M6

Table 65. EP20K1000E I/O Pins (Part 21 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	679	GNDINT	GND	GND	GND
–	680	VCCINT	VCCINT	VCCINT	VCCINT
8	681	I/O	G3	G8	M5
8	682	I/O	–	–	L8
8	683	I/O	G4	G3	L7
8	684	I/O	–	–	L6
8	685	I/O	–	–	L5
–	686	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	687	I/O	G5	G5	K8
8	688	I/O	–	–	K7
8	689	I/O	G6	D5	K6
8	690	I/O	–	–	K5
8	691	I/O	–	–	K4
–	692	GNDINT	GND	GND	GND
–	693	VCCINT	VCCINT	VCCINT	VCCINT
8	694	I/O	E2	F3	J8
8	695	I/O	–	–	J7
8	696	I/O	D1	E4	J6
8	697	I/O	–	–	J5
8	698	I/O	–	–	J4
–	699	GNDIO	GND	GND	GND
8	700	I/O	C1	F4	H7
8	701	I/O	–	–	H6
8	702	I/O	F4	F5	H5
8	703	I/O	–	–	H4
8	704	I/O	–	–	G7
–	705	GNDINT	GND	GND	GND
–	706	VCCINT	VCCINT	VCCINT	VCCINT
8	707	I/O	F5	E3	G6
8	708	I/O	–	–	G5
8	709	I/O	F6	E5	F6
8	710	I/O	–	–	F5
–	711	VCCIO	VCCIO8	VCCIO8	VCCIO8
–	712	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	713	I/O	–	A4	E6

Table 65. EP20K1000E I/O Pins (Part 22 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	714	I/O	–	B4	E5
1	715	I/O	–	A5	E4
–	716	GNDINT	GND	GND	GND
–	717	VCCINT	VCCINT	VCCINT	VCCINT
1	718	I/O	–	B5	D5
1	719	I/O	–	C6	C5
1	720	–	–	–	–
1	721	I/O, DATA5 *(9)*	E7	F6	A5
1	722	I/O	–	–	F7
1	723	I/O	D6	C5	E7
1	724	I/O	–	–	H8
1	725	I/O	B3	E6	G8
–	726	GNDIO	GND	GND	GND
1	727	I/O	C5	F7	F8
1	728	I/O	A2	A7	E8
1	729	I/O	B4	D6	D8
1	730	I/O	E8	D7	C8
1	731	I/O	D7	J11	B8
1	732	I/O	–	–	L9
1	733	I/O	C6	B7	K9
1	734	I/O	–	–	J9
1	735	I/O	A3	H10	H9
1	736	I/O	–	–	G9
–	737	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	738	I/O	–	–	F9
1	739	I/O, DATA4 *(9)*	B5	G9	B5
1	740	I/O	–	–	E9
1	741	I/O	E9	C7	D9
1	742	I/O	–	–	C9
1	743	I/O	A4	G10	B9
1	744	I/O	D8	E7	L10
1	745	I/O	C7	F8	K10
1	746	I/O	B6	C8	J10
1	747	I/O	A5	E8	H10
–	748	GNDIO	GND	GND	GND

Table 65. EP20K1000E I/O Pins (Part 23 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	749	I/O	D9	D8	G10
1	750	I/O	–	–	F10
1	751	I/O	E10	H11	E10
1	752	I/O	–	–	D10
1	753	I/O	C8	A9	C10
1	754	I/O	–	–	B10
1	755	I/O	–	–	L11
1	756	I/O, DATA3 *(9)*	B7	F10	A8
1	757	I/O	–	–	K11
1	758	I/O	A6	K12	J11
–	759	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	760	I/O	–	–	H11
1	761	I/O	D10	D9	G11
1	762	I/O	C9	F9	F11
1	763	I/O	E11	E9	E11
1	764	I/O	B8	G11	L12
1	765	I/O	A7	C9	K12
1	766	I/O	D11	G12	J12
1	767	I/O	–	–	H12
1	768	I/O	C10	B9	G12
1	769	I/O	–	–	–
1	770	I/O	B9	F11	F12
–	771	VCCINT	VCCINT	VCCINT	VCCINT
–	772	VCCINT	VCCINT	VCCINT	VCCINT
–	773	GNDINT	GND	GND	GND
–	774	GNDINT	GND	GND	GND
–	775	GNDIO	GND	GND	GND
1	776	I/O, DATA2 *(9)*	A8	J12	A9
1	777	I/O	–	–	–
1	778	I/O	C11	E10	E12
1	779	I/O	–	–	L13
1	780	I/O	B10	H12	K13
1	781	I/O	A9	D10	J13
1	782	I/O	E13	J13	H13
1	783	I/O	D13	C10	G13

Table 65. EP20K1000E I/O Pins (Part 24 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	784	I/O	C12	B10	F13
1	785	I/O	B11	E11	E13
1	786	I/O	–	–	D13
–	787	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	788	I/O	E14	D11	C13
1	789	I/O	–	–	B13
1	790	I/O	A10	D12	L14
1	791	I/O	–	–	K14
1	792	I/O	–	–	J14
1	793	I/O, DATA1 *(9)*	C13	K13	A10
1	794	I/O	–	–	H14
1	795	I/O	B12	A10	G14
1	796	I/O	–	–	F14
1	797	I/O	D14	E12	E14
–	798	GNDIO	GND	GND	GND
1	799	I/O	A11	A11	D14
1	800	I/O	E15	F12	C14
1	801	I/O	C14	H13	B14
1	802	I/O	B13	B12	L15
1	803	I/O	A12	B11	K15
1	804	I/O	–	–	J15
1	805	I/O	A13	D13	H15
1	806	I/O	–	–	G15
1	807	I/O	D15	A12	F15
1	808	I/O	–	–	E15
–	809	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	810	I/O	–	–	D15
1	811	I/O, CLKUSR *(9)*	C15	K14	A13
1	812	I/O	–	–	C15
1	813	I/O	E16	D14	B15
1	814	I/O	–	–	L16
1	815	I/O	B14	D15	K16
1	816	I/O, RDYNBSY *(9)*	A14	J14	A14
1	817	I/O	B15	C11	J16
1	818	I/O	A15	B13	H16

Table 65. EP20K1000E I/O Pins (Part 25 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	819	I/O	D16	C12	G16
–	820	GNDIO	GND	GND	GND
1	821	I/O, INITDONE *(9)*	C16	J15	A15
1	822	I/O	–	–	F16
1	823	I/O	B16	B14	E16
1	824	I/O	–	–	D16
1	825	I/O	A16	C14	C16
–	826	GNDINT	GND	GND	–
–	827	TDO *(6)*	C17	G13	A18
1	828	FAST2	B17	F13	A19
–	829	VCCIO	VCCIO1	VCCIO1	VCCIO1
–	830	VCCINT	VCCINT	VCCINT	VCCINT
–	831	VCCINT	VCCINT	VCCINT	VCCINT
–	832	GNDINT	GND	GND	GND
–	833	GNDINT	GND	GND	GND
1	834	FAST1	B19	H14	A20
–	835	NCEO *(6)*	C19	G14	A23
–	836	TRST *(6)*	D19	F14	A24
–	837	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	838	I/O	A20	A15	C17
2	839	I/O	–	–	D17
2	840	I/O	B20	B15	E17
2	841	I/O	–	–	F17
2	842	I/O	C20	C15	G17
–	843	GNDIO	GND	GND	GND
2	844	I/O	D20	B16	H17
2	845	I/O	A21	C16	J17
2	846	I/O	B21	J16	K17
2	847	I/O	A22	K15	L17
2	848	I/O	B22	G15	B18
2	849	I/O	–	–	C18
2	850	I/O	E20	L14	D18
2	851	I/O	–	–	E18
2	852	I/O	C21	E13	F18
2	853	I/O	–	–	G18

Table 65. EP20K1000E I/O Pins (Part 26 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	854	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	855	I/O	–	–	H18
2	856	I/O	D21	H15	J18
2	857	I/O	–	–	K18
2	858	I/O	A23	E14	L18
2	859	I/O	–	–	B19
2	860	I/O	A24	A17	C19
2	861	I/O	B23	F15	D19
2	862	I/O	C22	B17	E19
2	863	I/O	E21	D16	F19
2	864	I/O	A25	E15	G19
–	865	GNDIO	GND	GND	GND
2	866	I/O	D22	C17	H19
2	867	I/O	–	–	J19
2	868	I/O	B24	H16	K19
2	869	I/O	–	–	L19
2	870	I/O	C23	A18	B20
2	871	I/O	–	–	C20
2	872	I/O	–	–	D20
2	873	I/O	A26	G16	E20
2	874	I/O	–	–	F20
2	875	I/O	E22	E16	G20
–	876	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	877	I/O	–	–	H20
2	878	I/O	B25	J17	J20
2	879	I/O	C24	D17	K20
2	880	I/O	D23	F16	L20
2	881	I/O	E23	H17	E21
2	882	I/O	A27	B18	F21
2	883	I/O	B26	G17	G21
2	884	I/O	–	–	H21
2	885	I/O	C25	C18	J21
2	886	I/O	–	–	–
2	887	I/O	A28	F17	K21
–	888	GNDINT	–	–	–

Table 65. EP20K1000E I/O Pins (Part 27 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	889	VCCINT	VCCINT	VCCINT	VCCINT
–	890	VCCINT	VCCINT	VCCINT	VCCINT
–	891	GNDINT	GND	GND	GND
–	892	GNDINT	GND	GND	GND
–	893	GNDIO	GND	GND	GND
2	894	I/O	B27	D18	L21
2	895	I/O	–	–	–
2	896	I/O	C26	E17	E22
2	897	I/O	–	–	F22
2	898	I/O	D25	C19	G22
2	899	I/O	A29	F18	H22
2	900	I/O	B28	A20	J22
2	901	I/O	E25	B20	K22
2	902	I/O	C27	E18	L22
2	903	I/O	D26	D19	B23
2	904	I/O	–	–	C23
–	905	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	906	I/O	A30	G18	D23
2	907	I/O	–	–	E23
2	908	I/O	B29	C20	F23
2	909	I/O	–	–	G23
2	910	I/O	–	–	H23
2	911	I/O	C28	H18	J23
2	912	I/O	–	–	K23
2	913	I/O	E26	D20	L23
2	914	I/O	–	–	B24
2	915	I/O	D27	K18	C24
–	916	GNDIO	GND	GND	GND
2	917	I/O	A31	E19	D24
2	918	I/O	B30	F19	E24
2	919	I/O	C29	G19	F24
2	920	I/O	D28	A22	G24
2	921	I/O	A32	J19	H24
2	922	I/O	–	–	J24
2	923	I/O	E27	E20	K24

Table 65. EP20K1000E I/O Pins (Part 28 of 28)

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	924	I/O	–	–	L24
2	925	I/O	B31	C21	A25
2	926	I/O	–	–	B25
–	927	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	928	I/O	–	–	C25
2	929	I/O	A33	D21	D25
2	930	I/O	–	–	E25
2	931	I/O	C30	F20	F25
2	932	I/O	–	–	G25
2	933	I/O	D29	B22	H25
2	934	I/O	E28	E21	J25
2	935	I/O	B32	A23	K25
2	936	I/O	A34	B23	L25
2	937	I/O	C31	F23	E26
–	938	GNDIO	GND	GND	GND
2	939	I/O	B33	C22	F26
2	940	I/O	–	–	G26
2	941	I/O	D30	G23	E27
2	942	I/O	–	–	F27
2	943	I/O	E29	C23	A28

Table 66 shows configuration and power pin information for EP20K1000E devices in 652-pin BGA, 672-pin FineLine BGA, and 1,020-pin FineLine BGA packages.

Table 66. EP20K1000E Configuration & Power Pins (Part 1 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
MSEL0 *(6)*	U35	N21	J30
MSEL1 *(6)*	W35	N20	K30
NSTATUS *(6)*	AN17	AA13	AM14
NCONFIG *(6)*	W32	P21	R30
DCLK *(6)*	U3	N7	W3
CONF_DONE *(6)*	AM17	AA12	AM13
INIT_DONE *(8)*	C16	J15	A15
nCE *(6)*	U1	P6	AC3
nCEO *(6)*	C19	G14	A23
nWS *(9)*	M1	P9	C4
nRS *(9)*	N1	N10	D4
nCS *(9)*	P2	M9	D3
CS *(9)*	R2	T6	E3
RDYnBSY *(9)*	A14	J14	A14
CLKUSR *(9)*	C15	K14	A13
DATA7 *(9)*	M6	M10	B4
DATA6 *(9)*	L6	L8	A4
DATA5 *(9)*	E7	F6	A5
DATA4 *(9)*	B5	G9	B5
DATA3 *(9)*	B7	F10	A8
DATA2 *(9)*	A8	J12	A9
DATA1 *(9)*	C13	K13	A10
DATA0 *(6)*, *(10)*	U4	N6	V3
TDI *(6)*	W1	P7	AD3
TDO *(6)*	C17	G13	A18
TCK *(6)*	AN19	AA14	AM19
TMS *(6)*	AM19	AA15	AM20
TRST *(6)*	D19	F14	A24
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14	AM18, AM15, A19, A20
CLK1p	W34	P20	N30
CLK2p	U2	N8	Y3
CLK3p	Y34	M19	W30
CLK4p	T2	R6	P3

Table 66. EP20K1000E Configuration & Power Pins (Part 2 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
LOCK1 *(2)*	AA30	L21	AC30
LOCK2 *(2)*	AB6	U6	AK4
LOCK3 *(2)*	R31	L18	H30
LOCK4 *(2)*	AC6	W7	AK5
CLKLK_ENA *(6)*, *(7)*	W33	P16	P30
CLKLK_OUT1p	U31	AE23	AM29
CLKLK_OUT2p	Y3	T7	AH3
CLKLK_FB1p	Y32	AE20	AL28
CLKLK_FB2p	T4	U8	K3
DEV_CLRn *(8)*	T6	R9	H3
DEV_OE *(8)*	Y5	R8	AE3
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24	A2, B1, F1, F2, L1, L2, U1, U2, U3, AB1, AB2, AG1, AG2, AL1, AM2, AL6, AM6, AL11, AM11, AL17, AM17, AL22, AM22, AL27, AM27, AM31, AL32, AG31, AG32, AB31, AB32, T30, T31, T32, L31, L32, F31, F32, B32, A31, A27, B27, A22, B22, A16, B16, A11, B11, A6, B6
VCCIO1	C4, D5, E17	A6, J10, L12	A12, B12, A7, B7, A3
VCCIO2	E19, D31, C32	A13, K16, M14, A16	A30, A26, B26, A21, B21
VCCIO3	F30, F31, U30	A21, L17, N15	M31, M32, G31, G32, C32
VCCIO4	W30, AL31, AL32	N24, R16, U18	AK32, AF31, AF32, AA31, AA32
VCCIO5	AN32, AN33, AL19	T15, V17, AF21	AL21, AM21, AL26, AM26, AM30
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13	AM3, AL7, AM7, AL12, AM12
VCCIO7	AL3, AL4, W6	P12, T10, AF6	AA1, AA2, AF1, AF2, AK1
VCCIO8	U6, E3, E4	K9, M11, N3	C1, G1, G2, M1, M2
VCC_CKLK1 *(3)*	AA35	AF18	W24
VCC_CKLK2 *(3)*	W4	N11	Y9
VCC_CKLK3 *(3)*	T34	AC26	M24
VCC_CKLK4 *(3)*	R4	P10	P9
VCC_CKOUT1 *(5)*	U33	AF22	N24
VCC_CKOUT2 *(5)*	Y1	V7	AA9

Table 66. EP20K1000E Configuration & Power Pins (Part 3 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D18, D17, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12 M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, AF15	B2, B3, C2, C3, F3, F4, G3, G4, L3, L4, M3, M4, T1, T2, T3, AA3, AA4, AB3, AB4, AF3, AF4, AG3, AG4, AK2, AK3, AL2, AL3, AJ6, AJ7, AK6, AK7, AJ11, AJ12, AK11, AK12, AL16, AM16, AJ21, AJ22, AK21, AK22, AJ26, AJ27, AK26, AK27, AK30, AK31, AL30, AL31, AG29, AG30, AF29, AF30, AB29, AB30, AA29, AA30, U30, U31, U32, M29, M30, L29, L30, G29, G30, F29, F30, C30, C31, B30, B31, C26, C27, D26, D27, C21, C22, D21, D22, A17, B17, C11, C12, D11, D12, C6, C7, D6, D7
GND_CKLK1 *(3)*	Y30	AE18	V24
GND_CKLK2 *(3)*	W2	P11	V9
GND_CKLK3 *(3)*	T33, V35	AC25, N25	P24, P23
GND_CKLK4 *(4)*	R3	R10	T9
GND_CKOUT1 *(5)*	U32	AE22	T24
GND_CKOUT2 *(5)*	Y2	V6	W9

Table 66. EP20K1000E Configuration & Power Pins (Part 4 of 4)

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
No Connect (N.C.)			M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, N12, N13, N14, N15, N16, N17, N18, N19, N20, N21, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21
Total User I/O Pins *(11)*	488	508	708

Notes to tables:

(1) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for LVDS standard. If not used for the LVDS pair, these pins are regular I/Os. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(2) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) The CLKLK_OUT and CLKLK_FBIN pins are powered by the VCC_CKOUT and GND_CKOUT pins.

(5) This pin is the power or ground for the external output and feedback input of a PLL. These pins should be set to the V_{CCIO} level/standard desired for the external clock output and feedback input (if used). To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the V_{CCIO} and GND_{IO} pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will begin lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(8) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(9) This pin can be used as a user I/O pin after configuration.

(10) This pin is tri-stated in user mode.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 2.06 supersedes information published in previous versions.

Version 2.06 Changes

- Updated "Features..." section on page 1
- Updated "Functional Description" on page 9
- Updated "MegaLAB Structure" on page 10
- Updated "Logic Array Block" on page 11
- Added Tables 11, 12, 14, 15, 16, 26, 27, 28, and 29
- Updated Tables 1, 3, 4, 5, 6, 7, 13, 17, 19, 20, 23, 31, and 64
- Added *Note (1)* to Table 2
- Updated *Note (3)* for Tables 3 and 4
- Updated Figures 1, 25, 26, 29, and 33
- Updated "Advanced I/O Standard Support" on page 44
- Updated "SameFrame Pin-Outs" on page 45
- Added "MultiVolt I/O Interface" on page 46
- Updated "LVDS Support" on page 49
- Added "50/50 Duty Cycle" on page 50
- Updated "Operating Conditions" on page 57
- Updated *Notes (2)* and *(8)* for Table 32
- Changed title to Tables 52 and 53
- Updated Tables 55, 58, and 63
- Changed the note for pin `GND_CKLK4` from *Note (4)* to *Note (3)* for Table 64 on page 169

Version 2.05 Changes

- Updated high density information in "Features..." on page 1
- Updated EP20K1500E information in Table 1 on page 1
- Corrected pin count for EP20K400E, EP20K600E, EP20K1000E, and EP20K1500E 652-Pin BGA devices in Table 3 on page 4
- Added programmable delay chain information in Tables 9 and 10
- Updated programmable delay information in Figures 25 and 26
- Corrected parameter description for t_H in Table 35 on page 69
- Corrected timing information for $t_{OUTCOBIDIR}$ in Tables 48 and 50
- Corrected placement of selectable I/O standard input adder delay information in Table 51 on page 80
- Corrected `CLK1` and `CLK2` pin names in Tables 54, 55, and 56
- Corrected total I/O pin information for the EP20K200E 672-pin FineLine BGA device in Table 60 on page 118
- Corrected pin information for `DCLK` and `VCCIO8` in Table 62 on page 142

Version 2.04 Changes

- Added f_{MAX} timing information in Figure 37 and Tables 35 through 40
- Added I/O pin information for EP20K100E, EP20K200E, EP20K400E, EP20K600E, and EP20K1000E devices in Tables 57, 59, 61, 63, and 65
- Added configuration and power pin information for EP20K100E, EP20K200E, EP20K400E, EP20K600E, and EP20K1000E devices in Tables 58, 60, 62, 64, and 66
- Updated pin names throughout document

Version 2.03 Changes

The *APEX 20K Programmable Logic Device Family Data Sheet* version 2.03 contains the following changes:

- Corrected high density information in "Features..." on page 1
- Corrected I/O count information in Tables 3 and 4
- Updated I/O standard support information for APEX 20KE devices in Table 7
- Updated Figures 26, 29, and 30
- Updated information in "Advanced I/O Standard Support" on page 44
- Updated information in "ClockLock & ClockBoost Features" on page 48
- Updated notes for Table 14
- Added pin-out information for the EP20K100 324-pin FineLine BGA device in Table 54
- Added pin out information for the EP20K200 484-pin FineLine BGA device in Table 55
- Corrected `GNDIO` pin numbers for the EP20K200 208-pin RQFP device in Table 55
- Updated notes for Tables 54 and 55
- Added pin-out information for the EP20K400 672-pin FineLine BGA device in Table 56
- Minor textual changes throughout the document

Version 2.02 Changes

The *APEX 20K Programmable Logic Device Family Data Sheet* version 2.02 contains the following change: I/O pin counts were updated for the 672-pin FineLine BGA package in Table 4.

Version 2.01 Changes

The *APEX 20K Programmable Logic Device Family Data Sheet* version 2.01 contains the following changes:

- Corrected LE, RAM bit, and product-term macrocell count and added information in "Features..." on page 1
- Updated Tables 1, 4, 6, 7, 14, 18, 19, 30, 54, 55, and 56
- Updated the package options and I/O count in Table 3
- Added information to "Functional Description" on page 9
- Changed the chip-wide reset pin from CHIP_RSTn to DEV_CLRn on page 20
- Corrected the number of ESB output lines in "Embedded System Block" on page 29
- Added Quartus Complier information to "I/O Structure" on page 38
- Added information on the CTT I/O standard to "Advanced I/O Standard Support" on page 44
- Corrected the maximum V_{OL} value for 3.3-V low-level TTL output in Table 31
- Updated Figures 25 and 26
- Updated the arrangement of the APEX 20K I/O blocks in Figure 29

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